UNIVERSITY OF CALIFORNIA
IRVINE

CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

GRADUATE FELLOWSHIP PROJECTS PROGRESS REPORTS FALL 2005

PROJECTS

ALPHABETIZED ACCORDING TO STUDENT LASTNAME

STUDENT NAME	PROJECT TITLE	ADVISOR
ENIS AKAY	Achieving Full Diversity and Full Spatial Multiplexing Gain in MIMO Wireless LANs	ENDER AYANOGLU
JUN HO BAHN	Reconfigurable Forward Error Correction Engine	NADER BAGHERZADEH
HAMID ESLAMI	Implementation of Channel Emulator on FPGA	AHMED ELTAWIL
KRISHNA SRIKANTH GOMADAM	Adaptive Partially Coherent Multiuser MIMO Transceiver Design for Rapidly Time Varying Channels	SYED A. JAFAR
INANC INAN	MAC Algorithms for 802.11 Wireless LANs	ENDER AYANOGLU
VIPUL JAIN	Silicon-Based Low-Noise IC Design for Millimeter-Wave Wireless Communications Systems	PAYAM HEYDARI
SEYED JAVAD KAZEMITABAR	Cooperation in a Large Network	HAMID JAFARKHANI
SREENIVAS RAO KOLLU	Design of Practical LDPC Codes	HAMID JAFARKHANI
BYONG-MOO LEE	Signal Processing for Peak-to-Average Power Ratio (PAPR) Reduction and OBE Mitigation for MIMO-MC-CDMA Wireless Communication Systems	RUI DE FIGUEIREDO
SUDEEP PASRICHA	SOC Power Optimization Framework	NIKIL DUTT FADI KURDAHI
ERSIN SENGUL	Adaptive Modulation and Coding for Bit-Interleaved MIMO-OFDM Systems	ENDER AYANOGLU
SUDHIR SRINIVASA	Cognitive Radio – Opportunistic and Reconfigurable Communication with Distributed Side Information	SYED A. JAFAR
SUNDARAMAN SRIRAMKUMAR	Ultra Low Power (ULP) Silicon-Based Analog/Mixed Signal IC Design	PAYAM HEYDARI
AHMAD YAZDI	Design Techniques Toward a Full-Rate 40 Gb/s Transmitter in 0.18 μs	MICHAEL GREEN

Progress Report on MIMO Research: Fall 2005

Enis Akay, Advisor: Ender Ayanoglu
Center for Pervasive Communications and Computing
Department of Electrical Engineering and Computer Science
The Henry Samueli School of Engineering
University of California, Irvine
Irvine, California 92697-2625
Email: eakay@uci.edu

***Abstract*— During Fall 2005, we investigated the performance of bit interleaved coded multiple beamforming with OFDM (BICMB-OFDM) for frequency selective channels. We provide interleaver design criteria such that the resulting system achieves full spatial multiplexing of $\min(N, M)$ and full spatial and frequency diversity of NML for a system with N transmit and M receive antennas over L-tap frequency selective channels when an appropriate convolutional code is used. Simulation results show that BICMB-OFDM provides substantial performance gain when compared to the best spatial multiplexing systems.**

I. Introduction

The main goal of next generation broadband wireless communication systems is to provide high data rates while maintaining the robustness of the system. To this end, multi-input multi-output (MIMO) systems are known to provide significant capacity increase [1], and high diversity order. Space-time codes achieve high diversity without any channel state information (CSI) at the transmitter and without increasing the throughput [2]. A technique that provides high diversity and coding gain with the help of CSI at the transmitter is known as beamforming. Beamforming separates the MIMO channel into parallel subchannels. Therefore, multiple streams of data can be transmitted easily. Single beamforming (i.e., sending one symbol at a time) was shown to achieve the maximum diversity in space with a substantial coding gain compared to space-time codes [3]. If more than one symbol at a time are transmitted, then the technique is called multiple beamforming. For uncoded multiple beamforming systems, it was shown that while the spatial multiplexing increases, one loses the diversity order with the increasing number of streams used over flat fading channels [4].

Bit interleaved coded modulation (BICM) was introduced as a way to increase the code diversity [5], [6]. BICM has been deployed with OFDM and MIMO OFDM systems to achieve high diversity orders over frequency selective channels [7], [8]. During Fall 2005, we investigated bit interleaved coded multiple beamforming with OFDM. Our investigation concluded that with the inclusion of BICM using an interleaver satisfying certain design criteria, one does not lose the diversity order with multiple beamforming even when all the subchannels are used. That is, our work showed that BICMB-OFDM achieves full diversity NML, and full spatial multiplexing $\min(N, M)$ for a system with N transmit and M receive antennas over L-tap frequency selective channels, when an appropriate convolutional code is used. Spatial multiplexing is defined as the number of symbols transmitted simultaneously over N transmit antennas.

II. Simulation Results

In the simulations below, the industry standard 64-states, 1/2-rate, (133,171), $d_{free} = 10$ convolutional code is used. Coded bits are interleaved using the interleaver in [9], which satisfies the design criteria for the interleaver. The coded bits are mapped onto symbols using 16 QAM with Gray labeling. One packet has 1000 bytes of information bits. Each OFDM symbol has 64 subcarriers, and has 4 μs duration, of which 0.8 μs is CP. All the comparisons below are carried at 10^{-5} bit error rate (BER).

Figure 1 illustrates the results for BICMB-OFDM for different rms delay spread values, when 2 streams of data are transmitted at the same time. The maximum delay spread of the channel is assumed to be ten times the rms delay spread. Each tap of the frequency selective channel is assumed to have equal power. The channel is assumed to change independently from packet to packet. The spectrum of (133,171) shows that there are 11 codewords with an Hamming distance of d_{free} from all-zero codeword. When compared to all-zero codeword, the codeword [1110010100010101110000000...] has the worst performance for BICMB-OFDM. On this codeword $\alpha_1 = 3$, and $\alpha_2 = 7$. Consequently, when $S = 2$, BICMB-OFDM achieves a maximum diversity order of $3NM + 7(N-1)(M-1)$ (19 for 2×2 system). Note that, on Figure 1 up to rms delay spread of 15 ns, BICMB-OFDM achieves the maximum diversity with full spatial multiplexing of 2. 2×2 system over 20 ns channel provides a maximum achievable diversity order of 20. Therefore, BICMB-OFDM achieves a diversity order of 19 for rms delay spreads of 20 ns, 25 ns, and 50 ns.

Figures 2 and 3 illustrate the simulation results for BICMB-OFDM, BICM-OFDM with spatial multiplexing (BICM-SM-OFDM) using maximum likelihood decoding (MLD), minimum mean squared error receiver (MMSE), and zero forcing receiver (ZF). In both figures, the spatial multiplexing is set as two. The simulations are carried over IEEE channel models B, and D [10], [11], [12]. Note that BICMB-OFDM employs CSI at both the transmitter and the receiver while MLD, MMSE, and ZF employ CSI at the receiver. As can be seen, BICMB-OFDM outperforms significantly high complexity, but best

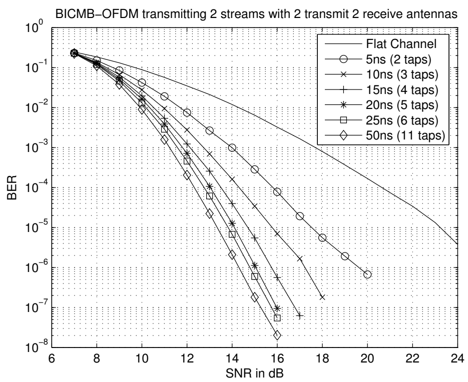

Fig. 1. BICMB-OFDM transmitting 2 streams using 2 transmit and 2 receive antennas.

spatial multiplexing receiver, MLD, by more than 3.5 dB. Note that, the decoding complexity of BICMB-OFDM is substantially lower in complexity than MLD. BICMB-OFDM outperforms easy-to-implement MMSE and ZF receivers by more than 10 dB and more than 15 dB, respectively. It is possible that the base station (or the access point) has more antennas than the receiver. BICMB-OFDM with 4 transmit and 2 receive antennas with spatial multiplexing of 2 outperforms MLD by 9 dB.

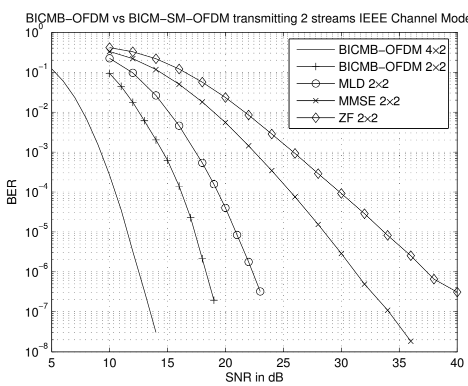

Fig. 2. BICMB-OFDM vs MLD, MMSE, and ZF transmitting 2 streams over IEEE Channel Model B.

Figure 4 presents the results for 4×4 case transmitting 4 streams for BICMB-OFDM, MMSE, and ZF over IEEE channel models B and D. BICMB-OFDM outperforms MMSE by more than 14 dB, and ZF by more than 22 dB.

In all the simulations presented in this section, it is assumed that the beamforming vectors are perfectly known at the transmitter. This may not be the case for a practical system, since it may require a high-speed feedback channel depending on the application. However, as shown in the figures, BICMB-OFDM provides a substantial gain when compared to current practical systems. This substantial gain is encouraging to investigate the limited feedback problem for a practical BICMB-OFDM system.

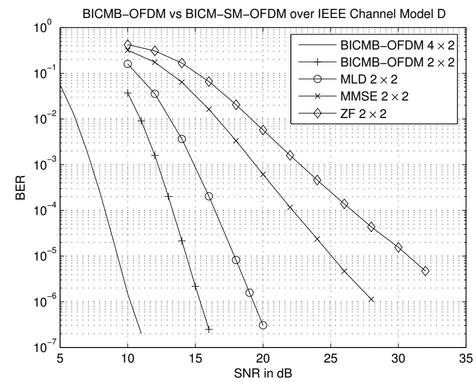

Fig. 3. BICMB-OFDM vs MLD, MMSE, and ZF transmitting 2 streams over IEEE Channel Model D.

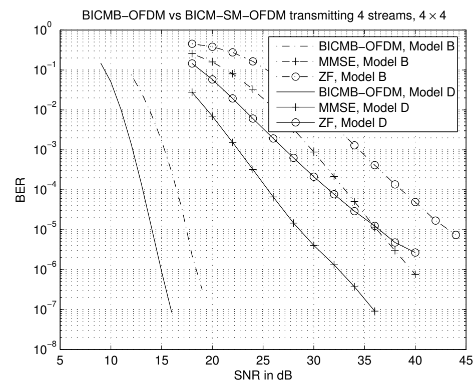

Fig. 4. BICMB-OFDM vs MMSE, and ZF transmitting 4 streams over IEEE Channel Models B, and D.

References

[1] G. Foschini and M. J. Gans, "On limits of wireless communcations in a fading environment when using multiple antennas," *Wireless Personal Communications*, vol. 6, no. 3, pp. 311–335, March 1998.

[2] H. Jafarkhani, *Space-Time Coding: Theory and Practice*. Cambridge University Press, 2005.

[3] E. Akay, E. Sengul, and E. Ayanoglu, "Performance analysis of beamforming for MIMO OFDM with BICM," in *IEEE ICC '05*, Seoul, Korea, May 2005, pp. 613–617.

[4] E. Sengul, E. Akay, and E. Ayanoglu, "Diversity analysis of single and multiple beamforming," in *Proc. IEEE VTC Spring '05*, Stockholm, Sweden, May 2005.

[5] E. Zehavi, "8-PSK trellis codes for a Rayleigh channel," *IEEE Trans. Commun.*, vol. 40, no. 5, pp. 873–884, May 1992.

[6] G. Caire, G. Taricco, and E. Biglieri, "Bit-interleaved coded modulation," *IEEE Trans. Inform. Theory*, vol. 44, no. 3, May 1998.

[7] E. Akay and E. Ayanoglu, "Full frequency diversity codes for single input single output systems," in *IEEE VTC Fall '04*, Los Angeles, USA, September 2004.

[8] ——, "Bit-interleaved coded modulation with space time block codes for OFDM systems," in *IEEE VTC Fall '04*, Los Angeles, USA, September 2004.

[9] WWiSE Proposal: High throughput extension to the 802.11 Standard. IEEE. [Online]. Available: ftp://802wirelessworld.com/11/04/11-04-0886-06-000n-wwise-proposal-ht-spec.doc

[10] J. P. Kermoal, L. Schumacher, K. I. Pedersen, P. E. Mogensen, and F. Frederiksen, "A stochastic MIMO radio channel model with experimental validation," *IEEE J. Select. Areas Commun.*, vol. 20, no. 6, pp. 1211–1226, August 2002.

[11] IEEE 802.11-03/940r2:TGn Channel Models. IEEE. [Online]. Available: ftp://ieee:wireless@ftp.802wirelessworld.com/11/03/11-03-0940-02-000n-tgn-channel-models.doc

[12] IST-2000-30148: Intelligent Multi-Element Transmit and Receive Antennas I-METRA. IST. [Online]. Available: http://www.ist-imetra.org/

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

GRADUATE FELLOWSHIP PROGRESS REPORT FALL 05

Project Name: Network-on-Chip Architecture in MaRS
CPCC Affiliate Professor: Prof. Nader Bagherzadeh
Address; Tel.; E-mail: Eng. Tower 544F, Irvine, CA, 92697-2625; 949-824-8720; nader@uci.edu
Student: Jun Ho Bahn
Date: January 12, 2006

Introduction: We introduced MaRS[1], a unique reconfigurable, parallel computing architecture with simple packet-based communication networks between each processing element (PE), providing capabilities of the computation-/data-intensive data processing such as multimedia processing and wireless communication applications. At the initial implementation, there were some limitations in global communication between the PEs in MaRS such as tightly coupled send/receive protocol to reduce out-of-order deliveries, insufficient control in group-PE communication, and other related issues. In this project, we propose some enhanced network facilities which are appropriate for VLSI implementation and have a reduced complexity, high throughput, and simple routing algorithm even if basic network problems such as deadlock, livelock, etc are considered. We develop a new packet definition to support such different requirement in MaRS and also verify its efficiency by comparing simulation results. By providing uniform way of constructing such network architecture, its scalability can be easily accomplished. And this network architecture can be applied to different SoC developments.

Summary of Accomplishments: In the Fall Quarter 2005, we defined some specification of Network-on-Chp (NoC) architecture in MaRS such as data formats, routing algorithms, router architectures, etc. We defined two different network data formats such as a packet-based data format and flit-based one. And as routing algorithms, we based on wormhole routing algorithms. We support both oblivious routing and minimal adaptive routing by changing the configuration parameters while controlling each router. For the purpose of functional verification of router architecture as well as performance evaluation, we are implementing each of router models in SystemC. Currently we assume a minimal adaptive routing algorithm in router architecture. Based on two different network data formats, we are implementing a template-based data format. We implemented one router model which supports a packet-based data format consisting of different types of transfer modes such as single/block transfer. It was tested in basic functionality and by constructing 2-dimensional mesh network its operation was verified from the point of source/destination PE (processing element). In parallel, we implemented a similar router model in HDL. With this model, we synthesized and estimated its hardware cost such as area, power and so on to check the feasibility. Currently we used the TSMC 0.18μ design library.

Regarding performance evaluation, it is important what kinds of test vectors are used. Generally there are two different types of approaches, random traffic generation and application specific traffic generation. In random traffic generation, while it can test various kinds of network traffic patterns in random manners, it requires over-estimated specifications like higher requirement of buffer size at each port in router. In reality, the application specific traffic generation approaches can compensate for such impracticality. At first, we developed random traffic generator for a packet-based data format. Currently we are looking for the requirement of parameters for controlling the random traffic generator such as range of destination PE to communicate with, traffic load, ratio of different traffic data types (single/block) and so on.

On going work: The other type of router model which supports a flit-based data format will be implemented in SystemC and be tested by applying similar ways of putting various test vectors. With the implemented router models and traffic generators, several experiments will be performed. For each router model, the performance analysis such as latency, congestion ratio, throughputs and rate of out-of-order delivery can be measured by varying the parameters. And depending on the type of data formats, we will analyze each performance and effect in network performance. Finally we will choose one of data formats for the NoC architecture in MaRS. With the experimental results and comparison we will prepare for some conference papers.
One of the issues is how to combine the random generation and application specific one. As our approach, we proposed a script-based methodology. In order to do that, we will continue each implementation of traffic generator in SystemC. And by collecting and analysing the parameters to be defined for controlling each type of traffic generation we will develop new script language for describing the traffic generation of either random data or application specific ones. In order to get higher processing capability, the processor model located in EU (execution unit) will be changed with OpenRISC core. For the high-level simulation in SystemC, the SystemC model of EU with OpenRISC will be implemented.

In the next phase of this project we are going to map Turbo and Viterbi algorithms on the MaRS architecture.

Reference:

[1] **N. Tabrizi et al., "***MaRS: a macro-pipelined reconfigurable system***," Proc. Comp. Frontiers, pp. 343 – 349, Apr. 2004**

UC Irvine Center for Pervasive Communication and Computing Graduate Fellowship Progress Report Fall 05

Project Name: Ultra High Speed Real-Time Channel Emulation
CPCC Affiliate Professor: Prof. Ahmed M. Eltawil
Address, Tel., e-mail: Eng. Tower 516F, Irvine, CA 92697; 949 824 0125
{aeltawil,heslami}@uci.edu
Student: Hamid Eslami
Date: Jan. 10, 2006

Introduction: The ability to emulate (in real time) a realistic wireless channel under controlled conditions in the lab is of utmost importance in designing and verifying the functionality of all wireless systems. This is becoming increasingly important with advent of high data rate wireless standards such as 802.11n, where due to wideband nature of the incoming signal, the computation load on both the hardware and software required to accurately represent the artifacts of the wireless channel increases exponentially. Our goal is to research and implement a prototype of a scalable and efficient emulation algorithm for advanced wireless communication standards.

Summary of the Accomplished Work: We partitioned the research problem into three phases. Phase one involved a comprehensive study of the available literature covering efficient channel emulation implementations. This phase was essential to understand the state of the art algorithms employed, as well as provide a base for progress to phase two, which is the architectural phase of the project. In phase two - which started in mid Fall- we studied the optimum partitioning of the algorithms between software running on the host computer and real-time hardware, with the target of maximizing the processed bandwidth, with minimum hardware complexity.

General purpose processors, while possessing the computational power to perform all the required processing are input/output limited and are therefore incapable of meeting the real-time requirements of the system. For that reason, we partitioned the non-real time task of generating the channel coefficients to the host program running of the PC. The raw data channel processing is processed completely in hardware.

The next step in the research program was to identify the most efficient implementation. We studied performing the emulation algorithm in both the time and frequency domain. Time domain emulation has been a popular trend so far due to the straight forward computations required for complex convolution. Nonetheless, excess number of operations per data sample renders it an inefficient algorithm for wideband systems. This motivated us to consider frequency domain transformations as a means of reducing complexity. In the frequency domain approach, an overlap-add FFT scheme is executed over the spectrum of the channel samples and buffered data and an IFFT is performed to recover the time domain signal. Although, this might seem to be a complicated algorithm, our initial complexity analysis indicate very promising results, specially if adaptive FFT are used versus fixed length FFT operations. In preliminary results, the number of required complex multiplications and additions were reduced by 35% compared to the conventional approach of time domain processing. To validate these performance numbers a system level simulation was setup and used to generate and test numerous channels including all channel realizations compliant to the 802.11n standard.

All above contributions have led to a paper, namely "Ultra High Speed Real-Time Channel Emulation on FPGA" that explains the design methodology as well as preliminary finding. This paper will be submitted to the Vehicular Technology Conference, Fall 2006.

The On-going Work: During the up-coming quarter we will focus on finalizing the architecture and getting an accurate estimate of the implementation complexity in preparation for phase three of the project, which will be the prototyping phase. In phase three, we will map our algorithm to an FPGA based board that will be tested in the laboratory to verify the real-time performance of the system.

UC Irvine Center for Pervasive Communications and Computing
Graduate Fellowship Progress Report Fall 05

Project: Adaptive Partially Coherent Multiuser MIMO Transceiver Design for Rapidly Time Varying Channels.

CPCC Affiliate Prof Syed Ali Jafar

Contact: ET 616E, University of California Irvine, CA 92697-2625

Phone/E-mail: (949)824 1684/syed@uci.edu

Student: Krishna Srikanth Gomadam

Date: Jan 12, 2006

Introduction: Mobility results in rapid fluctuations in the fading channel between the transmitter and the receiver. While pure coherent detection cannot be performed in a rapidly time varying channel due to difficulty in obtaining perfect channel estimate, non-coherent detectors suffer from significant performance penalty (usually 3-dB). Our work involves utilizing partial channel knowledge in rapidly varying channels to obtain performance gain over the best of coherent (non-ideal) and non-coherent detection.

Summary of Work

In [1], [3], we investigate the performance degradation of basic modulation schemes in a rapidly time varying channel using a first order auto-regressive channel model. Employing this model, we quantify the performance loss in coherent modulation schemes as a function of the channel variation rate and channel estimation frequency. We obtain partially coherent detectors for DPSK and FSK that utilize inaccurate channel estimate, whose quality is determined by the frequency of channel estimation. The maximum likelihood (M.L) detection rule for FSK modulation turns out to be a linear combination of coherent and non coherent detection rules. A tight upper bound is derived for the symbol error probability with this detector by exploiting the fact that, for any symbol duration the performance of this detector is superior to the best of coherent and non -coherent detection. A performance gain of about 2 dB is obtained over a wide range of SNR. We identify parameters that different modulation schemes are sensitive to and propose two adaptive schemes, intra-block adaptation and inter-block adaptation. Simulation results indicate substantial performance improvements. We evaluate the performance of modulation schemes in a time varying channel based on metrics such as BER, hard decision capacity and BLER (block error rate). We determine that non coherent FSK modulation which incurs spectral efficiency loss suits in scenarios where a very high Doppler shift is encountered.

In [2], we analyze the performance degradation due to rapidly time varying channel in a cooperative network. We demonstrate that, despite the symmetry, mobility of source affects the performance much more than the mobility of destination for both amplify and forward, and demodulate and forward relays. We also develop partially coherent detectors that take into account the mobility of the nodes. These detectors, mostly are hybrids of partially coherent and non coherent detectors. A gain of about 2 dB is obtained the best of coherent and non-coherent detectors in fast fading channels. As energy efficiency is one of the main objectives for pursuing cooperation, these hybrid detectors assume significance in fast fading scenarios.

Future work includes study of the impact of inaccurate channel statistic at the receiver and extensions to frequency selective channels.

References:

[1] K. Gomadam, S. A. Jafar, “Partially Coherent. Detection. in Rapidly Time Varying Channels”, Accepted at IEEE WCNC 06.

[2] K. Gomadam, S. A. Jafar, “Impact of Mobility on Cooperative Communication”, Accepted at IEEE WCNC 06.

Quality of Service (QoS) Provisioning in 802.11e Wireless LANs

Inanc Inan (Advisor: Ender Ayanoglu)
Center for Pervasive Communications and Computing, EECS Department
The Henry Samueli School of Engineering, University of California, Irvine
Irvine, California 92697-2625
Email: iinan@uci.edu

I. Introduction

We are in the process of designing an HCF control framework that will enable comprehensive QoS services in the future WLAN networks. This framework includes:

- An adaptive HCCA scheduler that can handle different multimedia application profiles, varying link layer buffer and wireless channel conditions efficiently
- A controller block adapting the EDCA parameters and the flow mappings to the transmission queues depending on the current channel conditions and network load
- Call admission control (CAC) units designed for EDCA and HCCA which handle the channel capacity effectively and satisfies the QoS requirements of variable bit rate (VBR) multimedia flows

II. Fall'05 Accomplishments

We have completed the design of a novel application-aware adaptive HCCA scheduling algorithm which is fully compliant with the specifications of IEEE 802.11e standard [1]. The approach used in the service scheduling is original in the sense that the proposed algorithm adapts service intervals, polling order, and transmission opportunities depending on the VBR multimedia traffic characteristics, flow directions, and instantaneous buffered traffic conditions. The extensive simulations carried out indicate the effectiveness of the algorithm in QoS provisioning for VBR multimedia traffic flows of a WLAN scenario composed of a QBSS. The proposed scheduler provides QoS guarantees with high channel utilization, negligible packet loss ratio and timely multimedia packet delivery. This work will be presented at the IEEE International Conference on Communications, June 2006 [2].

At the time of this writing, the official distribution of the public domain network simulator, ns-2 [3], only supports DCF in the IEEE 802.11 MAC layer. We previously have constructed a functioning IEEE 802.11e HCF MAC simulation module for ns-2.28 [4]. Moreover, ns-2 does not include the implementation of any wireless channel models other than a couple of abstract radio propagation modules. The accomplishments of Fall'05 include the implementation of AWGN channel in the simulator.

The performance of the proposed scheduler on AWGN channel is studied. The proposed scheduler has a number of specifications useful in mitigating channel noise effectively such as adapting the uplink service schedule regarding the TXOP requests from the QSTAs and basing the downlink service schedule on buffer occupancy at the QAP. These extensions make the failed data packets, retransmission of which cannot fit in the current TXOP, be retransmitted much sooner rather than waiting another fixed service interval as it is in previous proposals, resulting in smaller packet loss ratio, delay and jitter. We actually have simulation results that indicate the stated extensions improve the scheduling performance for AWGN channel with low SNR, although they are not included in [2] due to space limitations. In low SNR case, the proposed adaptive scheduler still provides significant improvement on the overall channel utilization when compared with the state-of-the-art HCCA multimedia schedulers (around 30%). The packet loss rate remains in the QoS limits while the other schedulers cannot satisfy the QoS requirements.

We also implemented a simple QAP controller block adapting the EDCA parameters depending on the observed average packet loss ratio of multimedia flows. The EDCA parameters specific to the QSTAs are periodically broadcasted via beacon frames. The approach in determining the MAC level packet loss ratio for multimedia flows is novel in the sense that QAP uses a cross-layer approach by using the RTP header sequence number field in calculation. The preliminary simulations show the effectiveness of the adaptation on the EDCA performance.

Having the applications dynamically tuning the scheduling parameters poses some challenges on admission control. An efficient CAC algorithm design is left as future work. It should be noted that using a fair admission control algorithm and accepting fewer number of flows than the proposed scheduler can actually deal with efficiently will not alter the improved HCCA performance. Effective HCCA scheduling will increase the EDCA bandwidth thus the best-effort QoS.

References

[1] *IEEE 802.11 WG. Draft Supplement to IEEE Standard 802.11: Medium access control (MAC) Quality of Service (QoS) Enhancements*, IEEE 802.11e Std. D11.0, October 2004.
[2] I. Inan, F. Keceli, and E. Ayanoglu, "An Adaptive Multimedia QoS Scheduler for 802.11e Wireless LANs," in *Proc. IEEE ICC '05*, May 2005, to be published.
[3] Network Simulator, ns-2. [Online]. Available: http://www.isi.edu /nsnam/ns
[4] I. Inan, "Design, Implementation, and Verification of an IEEE 802.11e HCF Simulation Model in ns-2.28," CPCC," Progress Report, Winter 2005.

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
GRADUATE FELLOWSHIP PROGRESS REPORT Fall 2005

Project Name: Silicon-based Low-Noise IC Design for Millimeter-Wave Wireless Communication Systems
CPCC Affiliate Professor: Payam Heydari
Address, Tel., e-mail; ET 644C, Irvine, CA, 92697-2625; (949)824-9324; payam@ uci.edu
Student: Vipul Jain
Date: January 12, 2006

Introduction:

The allocation of 7 GHz of unlicensed spectra (22-29 GHz and 57-64 GHz) by FCC has enhanced interest and research aimed at utilizing this resource for high data-rate wireless communication systems such as wireless personal area networks (WPANs), vehicular radars, imaging systems etc. Integrated circuits for these spectra have been implemented in compound semiconductor technologies, but at a prohibitive cost. A CMOS implementation has the capability of bridging the gap between millimeter-wave circuits research and the consumer market.

Summary of Accomplishments:

An essential constituent of this project is the design of homodyne or direct-conversion receivers. As a starting point in the understanding of the challenges and bottlenecks involved in millimeter-wave circuit design, a 22-29 GHz ultra-wideband receiver front-end has been designed in IBM 0.18 micron RFCMOS technology. The front-end consists of a low-noise amplifier and in-phase/quadrature (I/Q) mixers. The maximum over-all gain of the front-end is 22 dB and the minimum noise figure is 7 dB.

One of the main limitations in the design at these frequencies is the limited gain available from transistors, due to circuit operation close to f_T. Moreover, the dimensions of active and passive devices and interconnects become comparable to the wavelengths at these frequencies. Hence, transmission-line effects can not be neglected, and need to be modeled accurately with the aid of 3-D electromagnetic analysis tools. In addition, several test structures including transistors, spiral inductors and transmission lines need to be fabricated and measured in order to characterize their models for these spectra.

A novel low noise amplifier (LNA) has been proposed for ultra-wideband millimeter-wave wireless radios. The proposed LNA employing a s*ingle* transistor with on-chip neutralization has been designed and fabricated in IBM 0.18 um RFCMOS 6-metal process. It delivers a maximum power gain of 14 dB, minimum noise figure of 4.5 dB, improved input-output isolation and a larger gain-bandwidth product. The two-stage amplifier draws 40 mA from a 1.8 V supply. A neutralization circuit consisting of a differential inductor and a MOS varactor nullifies the detrimental effect of gate-drain parasitic capacitance C_{GD}, resulting in bandwidth improvement and noise-figure reduction.

Single-balanced I/Q mixers with output buffers have been designed for the 22-29 GHz front-end. The forward gain is 8 dB and the noise figure is 14 dB over the whole bandwidth.

The frequency synthesizer consists of a quadrature VCO, injection-locked and dynamic dividers, and a tri-state phase and frequency detector.

On-going/future work:

The LNA, mixer and LNA+mixer ICs designed in IBM 0.18 micron RFCMOS technology have been received from the foundry, and are yet to be tested. A 25.5 GHz frequency synthesizer has been designed and will be sent for fabrication in March 2006. A complete 22-29 GHz ultra-wideband receiver consisting of the LNA, I/Q mixers and the frequency synthesizer will be designed and sent for fabrication in March 2006. The experience and understanding gained out of these designs will then be employed to implement circuits for the 57-64 GHz band. New techniques and design methodologies are also being investigated to obtain circuit operation with high bandwidths.

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
GRADUATE FELLOWSHIP PROGRESS REPORT FALL 05

Project Name:	Cooperation in a Large Network
CPCC Affiliate Professor:	Prof. Hamid Jafarkhani
Address, Tel., e-mail;	ET 616c , Irvine, CA, 92697-2625 **;** (949) 824-1755; hamidj@uci.edu
Student:	Javad Kazemitabar
Date:	January 10, 2006

Introduction:

To combat channel degradation in wireless networks, it is common to apply diversity techniques, e.g. time diversity, space diversity, or etc. Time diversity techniques are not bandwidth efficient in genearal. Also, whenever there is size limitation, one cannot use space diversity techniques. In these conditions, a good substitue can be coopeative diversity[1].

Summary of Accomplishments:

During the past few months we studied the user cooperation systems. We recognized different protocols that harness user cooperation. Among those are distributed space-time and coded cooperation. Perhaps the most interesting work we studied was [2], where the authors propose protocls for Amplify and Forward and Decode and Forward relay channels. They also come up with curves that designate the upper bound of rate and diversity tradeoff. It is now known what is the best we can do in an amplify and forward channel.
It is not known what is the upper bound of rate-diversity tradeoff curve in a decode and forward relay channel. One needs to first find this bound and then propose a coding scheme that achieves this bound.

On going work:

There are several open problems in this area including the diversity multiplexing tradeoff of half-duplex decode and forward channels. Our current work is completely focused on this problem. We are finding the shortcomings of the current protocol that cannot achieve the whole degrees of freedom in the relay. After we are done with this work we would like to start looking at larger networks and figure out whether or not cooperation in all scenarios is useful. We want to simulate these scenarios via computer simulations and then, based on those results study the laws ruling large networks.

References:

[1] A. Sendonaris, E. Erkip, and B. Aazhang, “User Cooperation Diversity-Part I and II,” *IEEE Trans. Comm.,* Nov. 2003.

[2] K. Azarian, H. Elgamal, and P. Schniter, “On the Achievable Diversity-Multiplexing Tradeoffs in Half-Duplex Cooperative Channels,” *IEEE Trans. Inform. Theory*, Dec. 2005.

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING GRADUATE FELLOWSHIP PROGRESS REPORT – FALL 05

Project Name: Design of Practical LDPC Codes
CPCC Affiliate Professor: Prof. Hamid Jafarkhani
Address: 616 C, Engineering Tower, Irvine, CA 92697-2625
Tel., E-mail: (949) 824-1755; hamidj@uci.edu
Student: Sreenivas Kollu
Date: 1/13/06

Introduction: Techniques like Density Evolution and extrinsic information transfer (EXIT) charts can be used to analyze the decoding of Low-Density Parity-Check (LDPC) codes when the block length is large. This analysis helps to design degree profiles for optimum convergence threshold. Unlike large block length codes, medium block length codes have an error floor. We are trying to extend the analysis tools to analyze medium sized codes and study the effects of degree profiles on convergence threshold and error floor.

Summary of Accomplishments: In [1], we analyzed the technique of designing irregular LDPC codes for large block lengths using extrinsic information transfer (EXIT) charts. We presented an analysis on the accuracy of EXIT charts for LDPC codes. Since then, we have investigated the possibility of extending the EXIT chart analysis for codes of practical block lengths like 2048 bits. We defined a parameter similar to mutual information as the tracking parameter in EXIT chart analysis. For medium block lengths, we have shown using simulations that these EXIT functions can be modeled as random functions. The expectation of this EXIT function is the mutual information transfer function of the code and the variance is inversely related to block length. This EXIT chart acts as a visualization tool for the decoding trajectories. From the decoding trajectories for the cases when the decoder does not converge, we can identify the bottle neck points on the EXIT chart.

On-going Work: We have made very good progress in this project and have identified important problems. We also have a good idea how to proceed. Unfortunately, due to some family issues, the student, Sreenivas, has applied for a leave of absence and will not be available for a while. We hope that as soon as the student is back, we can continue the project.

References:

[1] S. Kollu and H. Jafarkhani, "On the EXIT Chart Analysis of Low-Density Parity-Check Codes", *IEEE Global Communications Conference*, Nov. 2005.

Project Name: Signal Processing for Peak-to-Average Power Ratio (PAPR) Reduction and OBE Mitigation for MIMO-OFDM-Wireless Communication Systems
CPCC Affiliate Professor: Prof. Rui J.P. de Figueiredo
Mailing Address: Engineering Tower 616F, Irvine, CA, 92697-2625
Phone: (949) 824-7043
E-mail: rui@uci.edu
Student: Byung Moo Lee
Date: January 10, 2006

Background: It is well-known that one of the major problems of Orthogonal Frequency Division Multiplexing (OFDM) system is its high Peak-to-Average Power Ratio (PAPR) which seriously limits the linear dynamic range of the High Power Amplifier (HPA). Thus far, several PAPR reduction techniques for OFDM system have been proposed in the literature. Amongst them, the Partial Transmit Sequence (PTS) technique which was developed by Muller and Huber constitutes a promising approach to reduce PAPR in OFDM communication systems since it does not cause any signal distortion. However, a major problem of the PTS based technique is its very high complexity. In the Summer 2005 report, we stated that we are developing an Enhanced Iterative Flipping (EIF) algorithm to efficiently reduce the complexity of the PTS based PAPR reduction technique [1].

Summary of accomplishments: In the Fall Quarter of 2005, we have been developing a specific new version of the low complexity PTS based technique mentioned above. We call this version Tree-PTS (T-PTS) technique [2]. The T-PTS technique constitutes a totally different approach from EIF-PTS technique which we reported last summer. For this purpose, for a representative low complexity PTS based PAPR reduction technique, we can choose Cimini and Sollengerger's iterative flipping algorithm. However, there is still some performance gap between the iterative flipping algorithm and optimum PTS technique. In Cimini and Sollenberger's iterative flipping algorithm, even if we choose a phase factor which shows minimum PAPR in the first sub-block, that is not necessarily true when we reach the second or M^{th} sub-block where M is the number of sub-blocks. That is, if we choose another phase factor in the first sub-block which does not have minimum PAPR, rather than choose a phase factor which shows minimum PAPR, it is also possible that the PAPR of the signal would be smaller in the second or M^{th} sub-block. For this reason, we should keep more information rather than discard the information which does not show minimum PAPR at the current sub-block. If we keep all of information until the end sub-block, that would be the case of the ordinary PTS. If we only keep the one which shows minimum PAPR at each subblcok, that would be the case of Cimini and Sollenberger's iterative flipping algorithm. The important point to note is that the more information we keep, the better performance we get but with higher complexity. As a compromise between these two extremes, we have introduced two new adjustable parameters, which we call S and T. One of the initial simulation results is shown in Fig.1. In this simulation, we used 16-QAM/64-sub-carrier- OFDM with an over-sampling factor 4, divided one OFDM block into 4 sub-blocks, and used 4 phase factors to reduce PAPR of OFDM signals. More complete complexity and performance analysis is under study [3]

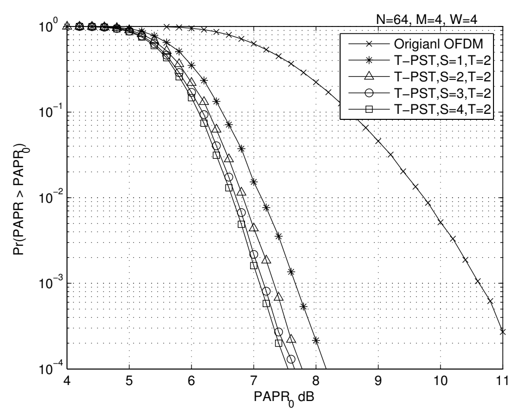

Fig.1. Initial simulation result of T-PST technique

References:

[1] Byung Moo Lee and Rui J.P. de Figuieredo, "An Enhanced Iterative Flipping Algorithm for PAPR reduction of OFDM signals" *In preparation for submission.*

[2] Byung Moo Lee and Rui J.P. de Figuieredo, "A Low Complexity Tree Algorithm for PTS-Based PAPR Reduction in Wireless OFDM" *(Accepted) to appear in ICASSP06, Toulouse, France, May 14 -16, 2006.*

[3] Byung Moo Lee and Rui J.P. de Figuieredo, "A Low Complexity Tree-PTS Technique for PAPR Reduction of Multicarrier Communication Systems" *In preparation for submission*

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
CPCC Fellowship Fall Quarter Progress Report, Jan 2006

Project Name: **SOC Power Optimization Framework**
Graduate Student: **Sudeep Pasricha**, ICS (on CPCC Fellowship for Fall 2005)
CPCC Affiliate Professors: **Nikil D. Dutt** and **Fadi J. Kurdahi**

Project overview

The long term goal of the proposed project is to develop a system level methodology for power optimization for SoCs. In the immediate term, the proposed project will investigate techniques for efficient power modeling of SOC bus architectures, as well as of system-level IP blocks, and their use in the architectural exploration of IP-based SOC designs. On the basis of such power models of the system, we will be able to explore the architectural design space and evaluate various scheduling schemes. Meanwhile, the model is designed to be easily refined as the design process goes through the design flow, providing more accurate estimating of system performance and power consumption. The major purpose of the model is to provide a vehicle for researches on power optimization, such as the HAIM/DOSE (Hierarchically Abstracted IP modeling by Data Organization Space Exploration) exploration flow proposed earlier. The model and exploration flow are based on the COMMEX transaction-level communication architectural framework, on which we will study the H.264 application (the latest video coding standard), and JPEG2000 (the latest still image coding standard).

Progress

During Fall 05, we engaged five students in this project and made good progress. The CPCC Fellow, Sudeep Pasricha, was aided by Yun Long, and together they focused on the SystemC modeling framework design as well as a case study of the H.264 decoder. Michael Shimaski worked on the on the RTL design of the H.264 Intra-Prediction module. Luis Bathen worked on JPEG2000 encoder modeling. Youg-Hwan Park worked on the ASIC design task with the goal of providing us with important implementation data, as well as taking over Yun Long's work, who will be graduating at the end of the quarter. During the fall quarter, we accomplished the following:

- Finished Sysplore tool chain based on Sysplore v0.2 developed in Summer 05. The added tools parse the configuration file as well as an optional module delay data file, and generate the Visual C++ project files, dummy C++ module files, and necessary macro definition files. Those files comprise a start-up Sysplore project that is immediately executable with automatically generated example data communication function calls and a default data-flow based system scheduler. This tool chain, together with the Sysplore v0.2 library, comprises the complete system modeling flow under SystemC.
- Updated Sysplore v0.2 to support FIFO, multi-layered AMBA APB bus protocol, and two types of memories: AMBA bus client memory and shared local memory. A demo suite is developed to demonstrate the design exploration on different channel types, memory types, and module implementation alternatives by simply modifying the system configuration file and the module delay data file. All these tests are also applied to the H.264 decoder case study, which has shown very interesting design tradeoffs.
- Work is in progress on the RTL design of the H.264 Intra-Prediction module. The first phase involved writing a detailed specification of the module and the steps needed to carry out the design. After writing the specification, coding of the module began in VHDL, and then switched to Verilog since most of the RTL designers in our group were using Verilog. Currently work is in progress on the final stage of running additional tests on the module. Our future work includes the implementation of the rest of the system design, alternative module design for certain modules, and processor model incorporation. This is a long-term task in parallel with our efforts on high-level modeling and optimization.

Going forward, our goal in 2006 is to finish the System model, integrating it with the performance and power data acquired from the ASIC design task, and study power optimization techniques with the help of easy design configuration of the model and accurate power modeling. The model should allow for easy and rapid migration to any multimedia application system.

One technical report was published during this period, and two papers were prepared and submitted to major conferences in the area (ASPDAC-2006 and DATE-2006). The publications are listed below.

Publications

1. Sudeep Pasricha, Nikil Dutt, "COSMECA: Application Specific Co-Synthesis of Memory and Communication Architectures for MPSoC", *Submitted to Design Automation and Test in Europe Conference (DATE 2006)*
2. Sudeep Pasricha, Nikil Dutt, Mohamed Ben-Romdhane, "Constraint-Driven Bus Matrix Synthesis for MPSoC", *Submitted to Asia and South Pacific Design Automation Conference (ASPDAC 2006)*
3. Sudeep Pasricha, Nikil Dutt, and M. Ben-Romdhane, "Bus Matrix Communication Architecture Synthesis," *CECS Technical Report 05-13, October 2005*

Progress Report on MIMO Research: Fall 2005

Ersin Sengul, Advisor: Ender Ayanoglu
Center for Pervasive Communications and Computing, EECS Dept.
The Henry Samueli School of Engineering, University of California, Irvine
Email: esengul@uci.edu

***Abstract*— We analyzed adaptive bit interleaved coded multiple beamforming (AMC-BICMB) with the inclusion of adaptive modulation and coding over flat fading channels. Our aim is to exploit the channel state information further and achieve superior throughput performance compared to BICMB and the other spatial multiplexing techniques in the literature. Simulation results show that AMC-BICMB achieves significant performance gain compared to uniform BICMB.**

I. Introduction

In recent years deploying multiple transmit and receive antennas has become an important tool to improve the capacity and robustness of wireless communication systems [1]. In order to combat the severe conditions of wireless channels, wireless systems should achieve a high diversity order. On the other hand, the increasing demand for high data rate communications requires high throughput. Practical schemes give up the essential diversity that is needed for better error performance in exchange of higher data rates. Designing new MIMO systems that can achieve both throughput and diversity gains simultaneously is one of the key issues in wireless communications.

Multi-input multi-output (MIMO) systems allow significant diversity gains in fading environments. Some of the MIMO systems incorporating diversity requires the channel state information (CSI) at the receiver, but not at the transmitter, e.g. space-time codes (see [2]). One other group requires perfect or partial CSI at both the transmitter and the receiver. When perfect CSI is available at both ends, beamforming can be used to maximize the SNR at the receiver. Beamforming separates the MIMO channel into parallel independent subchannels via Singular Value Decomposition (SVD). In the context of SVD-based beamforming, more than one subchannel can be used to improve the throughput. This technique is called multiple beamforming [3], [4].

We previously showed that the diversity order of uncoded multiple beamforming decreases as more symbols are transmitted simultaneously [4]. The recent results in [5] show that if a properly designed bit interleaved coded modulation (BICM) is incorporated to the SVD-based multiple beamforming, one can achieve full spatial multiplexing of $\min(N, M)$ and full spatial diversity of NM for N transmit and M receive antennas over flat fading channels. However, bit interleaved coded multiple beamforming (BICMB) of [5] employs uniform power and constellation over the established subchannels. As a result, BICMB does not fully utilize CSI at the transmitter. In this work, we further exploit CSI with the inclusion of adaptive modulation and coding (AMC) in the system and maximize the throughput keeping the power level constant with a target bit error rate (BER). Adaptive coding [6], adaptive modulation [7], and AMC [8], were previously analyzed for different systems and their results show that significant gains can be achieved compared to non-adaptive coded case.

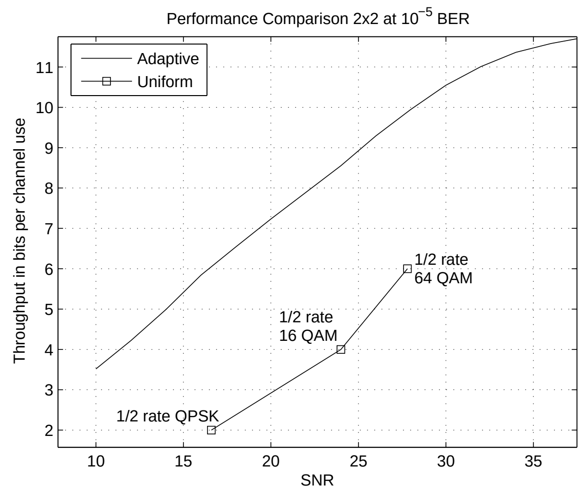

Fig. 1. Throughput performance of AMC-BICMB and uniform BICMB for 2×2 antenna configuration at 10^{-5} BER.

Some of our findings will appear in the proceedings of IEEE VTC Spring 2006 conference [9] and also in a journal paper to be submitted to the IEEE Transactions on Wireless Communications.

II. Simulation Results

In the simulations below, the industry standard 64 states 1/2 rate (133,171) $d_{free} = 10$ convolutional code is used as the mother code. The rates $2/3$ and $3/4$ are constructed from the 1/2 rate mother code via puncturing. Therefore the cardinality of the encoder set used for adaptive loading is 3. The minimum Hamming distances are 10, 6 and 5 for the encoders respectively. For the high SNR region, we also allow uncoded adaptive loading to achieve rate 1, where the minimum Hamming distance is 1. The channel is assumed to be quasi-static and flat fading with Rayleigh distribution.

In Fig. 1, the throughput performance of AMC-BICMB is compared with that of BICMB which uses uniform power and constellation over the established subchannels by multiple beamforming for the 2×2 case. The throughput definition used in the figure corresponds to the average number of information bits transmitted per each channel use. For BICMB, we used 3 different modes to plot its throughput curve which are 1/2 rate QPSK, 16 QAM and 64 QAM. For these 3 modes, BICMB achieves the target of 10^{-5} BER with transmitting 2 streams (equivalently 2 symbols simultaneously). The performance gain of AMC-BICMB is 11-13 dB compared to uniform BICMB, which is significant.

REFERENCES

[1] G. Foschini and M. J. Gans, “On limits of wireless communcations in a fading environment when using multiple antennas,” *Wireless Personal Communications*, vol. 6, no. 3, pp. 311–335, March 1998.

[2] H. Jafarkhani, *Space-Time Coding: Theory and Practice*. Cambridge University Press, 2005.

[3] D. P. Palomar, “A unified framework for communications through MIMO channels,” Ph.D. dissertation, Universitat Politecnica de Catalunya, Barcelona, Spain, May 2003.

[4] E. Sengul, E. Akay, and E. Ayanoglu, “Diversity analysis of single and multiple beamforming,” in *Proc. IEEE VTC Spring ‘05*, Stockholm, Sweden, May 2005.

[5] E. Akay, E. Sengul, and E. Ayanoglu, “Bit interleaved coded multiple beamforming,” to appear in the proceedings of IEEE WCNC 2006.

[6] B. Vucetic, “An adaptive coding scheme for time-varying channels,” *IEEE Trans. Commun.*, vol. 39, pp. 653–663, May 1991.

[7] A. Goldsmith and S. . Chua, “Variable-rate variable-power MQAM for fading channels,” *IEEE Trans. Commun.*, vol. 36, no. 4, pp. 389–400, April 1997.

[8] K.-B. Song, A. Ekbal, S. Chung, and J. M. Cioffi, “Adaptive modulation and coding (AMC) for bit-interleaved coded OFDM(BIC-OFDM),” in *Proc. IEEE ICC ‘04*, Paris, France, June 2004.

[9] E. Sengul, E. Akay, and E. Ayanoglu, “Adaptive modulation and coding for bit interleaved coded multiple beamforming,” to appear in the proceedings of IEEE VTC Spring 2006.

UC Irvine Center for Pervasive Communications and Computing

Graduate Fellowship Progress Report (Fall 2005)

Project name:	Cognitive Radio - Opportunistic and Reconfigurable Communication with Distributed Side Information
CPCC Affiliate Professor:	Prof. Syed Ali Jafar
Mailing Address:	ET 616E, University of California Irvine, CA, 92697-2625
Phone, E-mail:	(949)824-1684; syed@uci.edu
Student:	Sudhir Srinivasa
Date:	Wednesday, 11 January 2006

Introduction: Cognitive radios are encouraging solutions to improve the utilization of the radio spectrum - a finite and valuable resource. Their advantages are a direct result of the radios' ability to monitor the radio spectrum, intelligently detect occupancy in different segments of the spectrum and then opportunistically communicate over unused segments (spectrum holes) without interfering with the transmissions of the licensed (primary) users. The capacity of a cognitive user in a distributed and dynamic spectral environment is a measure of the ultimate performance limits of cognitive radios.

Summary of Accomplishments: In the past quarter, we have submitted two [1, 2] conference papers. [1] was submitted to the IEEE International Communications Conference (ICC 2006) and has been accepted for publication. [2] has been submitted to the IEEE International Symposium on Information Theory (ISIT 2006) and is currently under review. We are also preparing the journal versions of both the above papers for submission.

In [1], we explore the capacity limits of opportunistic communication in the presence of dynamic and distributed spectral activity, i.e. when the time varying spectral holes sensed by the secondary(cognitive) transmitter and receiver are not identical but correlated with each other. Developing a switch model for the cognitive system we derive capacity expressions with both causal and non causal side information at the transmitter and/or receiver. Lower and upper bounds on the capacity are also presented to complement the capacity results. We use the capacity expressions derived to determine the value of side information and the necessity of the overhead associated with the handshake between the transmitter and receiver to initiate opportunistic communication. With numerical results, we investigate the benefit of the handshake overhead for both lightly loaded and heavily loaded systems. We find that while the capacity benefits of overhead information flow from the transmitter to the receiver is very small, feedback information overhead in the opposite direction provides significant throughput improvements. Our numerical results also establish that cognitive radio communication is robust to dynamic spectral environments even when the communication occurs in bursts of only 3-5 symbols.

[2] considers a cognitive system operating on a spectrum pool of two frequency bands owned by primary users with independent and identical occupancy distributions. We model the primary user occupancies in the two channels with identical Markov processes. The secondary transmitter monitors both the channels (frequency bands) and chooses an unoccupied channel (if any) based on a transmitter policy. On the other hand, the receiver is constrained to be able to monitor only a single channel during any time slot and hence has to judiciously track the transmitter state and choose the channel to monitor for secondary signals. We seek to determine the receiver strategy that maximizes the capacity obtainable by the secondary user. Since the mutual information formulation for this model is not very analytically tractable, we approach the problem through the notion of matching probability, the probability that the transmitter and receiver are matched to the same channel. We bound the capacity of the system by deriving tight upper and lower bounds on the matching probability which are then used to bound the system capacity.

On going work: In [1, 2] we have developed simple yet representative models for cognitive radio systems. The theoretical framework is being extended to include additional considerations like missed primary user detection, fading channels and multi-secondary user interference. Furthermore, we are also analyzing the capacity of the cognitive system in the wideband limit.

References:

[1] S. A. Jafar and S. Srinivasa, "Capacity limits of cognitive radio with distributed and dynamic spectral activity," *IEEE International Conference on Communications*, June 2006.

[2] S. Srinivasa and S. A. Jafar, "On the capacity of the cognitive tracking channel," *Submitted to IEEE International Symposium on Information Theory*, 2006.

GRADUATE FELLOWSHIP PROGRESS REPORT Fall 2005

Project Name: Ultra-Low Power (ULP) Silicon-Based Analog/Mixed-Signal IC Design
CPCC Affiliate Professor: Payam Heydari
Address, Tel., e-mail; ET 644C, Irvine, CA, 92697-2625; (949)824-9324; payam@uci.edu
Student: Sriramukar Sundararaman and Amin Shameli
Date: January 11, 2006

Introduction:

The ever increasing complexity of wireless communication transceivers makes the power minimization of accompanying RF front-end one of the most important design objectives. In particular, power minimization becomes crucial in emerging technologies such as body implanted sensors, radio frequency identification systems (RFID), and sensor networks, all of which requiring power consumption in microwatt range in order to enable the constituent transceiver to operate either without integrated power supply or at an extremely long battery-life.

Summary of Accomplishments:

We have made a significant progress since the start of the project. *The project will radically change the way low-power circuits are designed*. Result of our investigation was submitted to IEEE RFIC symposium 2006. This paper investigates the use of CMOS technology to implement the ultra-low power (ULP) RF integrated circuits [1].

Due to its high integration capability and its continuously scaled feature size, nanoscale CMOS technologies remain a prime candidate for the future developments of ultra-low power (ULP) integrated circuits. Additionally, an extensive prior research on CMOS ULP digital IC design has laid the groundwork to design micropower baseband system in CMOS technologies. Heavily supported by the concept of system-on-chip (SOC), the design of ULP RFICs in CMOS technologies, however, entails several design challenges.

One of the main limitations in the ULP CMOS RFIC design is the low value of transistor's transconductance, g_m, due to the low bias current. Having already examined in low-power analog/digital ICs, an effective way of minimizing power consumption is to bias the transistor(s) in weak inversion region where the transistors achieve maximum value of g_m/I_D [2], [3]. Nonetheless, a weakly inverted transistor exhibits poor frequency response, and therefore, may not be used extensively in RFIC design.

In our paper we studied the use of moderately inverted MOS transistors in ultra-low power (ULP) RFIC design. We introduced a new figure of merit for a MOS transistor, i.e., the $g_m f_T$-to-current ratio, ($g_m f_T/I_D$), which accounts for both the unity-gain frequency and current consumption during the optimization process of the transistor's performance. Using this figure of merit while taking into account the velocity saturation of short-channel MOS devices, it has been shown both experimentally and analytically that the $g_m f_T/I_D$ reaches its maximum value in moderate inversion region. Moreover, we analytically investigated the noise behavior of the MOS transistor during the transition from weak inversion to strong inversion region. The measurement results have been obtained for an NMOS transistor fabricated in Jazz Semiconductor's CMOS 0.18µm process.

In addition, a novel Low Noise Amplifier (LNA) has been designed and fabricated for the proposed ULP RF radio. A differential inductor feedback doubles the LNA's gain and neutralizes the C_{GD} effect using a neutralizing capacitor C_N. The input device is biased to operate in an unconventional region, i.e., moderate inversion region, to achieve microwatt power dissipation. Moreover, the proposed LNA employs an active transistor to improve the gain. Preliminary results indicate a record-breaking power dissipation of 75µW, a noise-figure (NF) of 3.5dB, and a forward gain of 21dB. The circuit is designed and sent for fabrication using Jazz Semiconductor's CMOS 0.13µm process.

On going work:

As a continuation of our project, we are going to design and implement the whole ULP radio. Also we are investigating new communication techniques that enable the power dissipation to be reduced even more.

References:

[1] Amin Shameli, Payam Heydari, "Ultra-Low Power RFIC Design Using Moderately Inverted MOSFETs: An Analytical/Experimental Study" *submitted to IEEE RFIC Symposium 2006.*

[2] F. Silveira, D. Flandre, P. G. A. Jespers, "A g_m/I_D Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA," *IEEE J. of Solid-State Circuits*, vol. 31, no. 9, pp. 1314-1319, Sep. 1996.

[3] D. J. Comer, D. T. Comer, "Using the Weak Inversion Region to Optimize Input Stage Design of CMOS Op Amps," *IEEE Trans. on Circuit and Systems-II*, vol. 51, no. 1, pp. 8-14, Jan. 2004.

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
GRADUATE FELLOWSHIP PROGRESS REPORT SPRING 2005

Project Name:	Design Techniques Toward a Full-Rate 40Gb/s Transmitter in 0.18μm CMOS
CPCC Affiliate Professor:	Michael Green
Mailing Address:	544 Engineering Tower, Irvine, CA, 92697-2625
Phone:	(949) 824-1656
E-mail:	mgreen@uci.edu
Student Fellowship Recipient:	Ahmad Yazdi

Introduction: Many bandwidth enhancement techniques have been developed to increase the speed of the CMOS ICs. We combined the distributed and lumped techniques to push the technology to the its limit, enabling CMOS technology operating at 40Gb/s.

Summary of Accomplishment: Design of the 40Gb/s 50Ω driver with sufficient output amplitude is one the major challenges in this technology. The conventional tapered buffer does not have enough bandwidth for 40Gb/s speed. On the other hand, a single CML buffer with 50Ω load does not have enough gain to drive 50Ω. We design a distributed buffer with 50Ω characteristic impedance on the drain line while having a 100Ω characteristic impedance on the gate line. This distributed buffer is driven by an open drain CML buffer [1] where a broadband matching network has been applied to the input of the gate line in order to reduce the output jitter. A 40GHz differential push-push VCO has already been designed. To drive the 40Gb/s retimer a tuned buffer with shunt peaking has been implemented. Simulation shows that at such a high frequency shunt peaking with tuned buffer provides extra peaking at 40GHz, which results in a high amplitude clock.

On going Work:

1. **Design of the PLL** : A PLL with 2.5GHz input clock will be designed to complete the CMU of the transmitter.

2. **Top Level Simulation**: Connecting the CMU to the Multiplexer and runing the top level simulation.

3. **Post Layout Simulation**: Post layout simulation with RCX for high speed blocks and EM verification of the 40GHZ and 20GHz nodes in CMU.

References

[1] Singh, U.; Lijun Li; Green, M.M, "A 34Gb/s 2:1 MUX/CMU based on a distributed amplifier using 0.18μm CMOS" *VLSI Circuits, Digest of Technical Papers* June 2005