UNIVERSITY OF CALIFORNIA
IRVINE

CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

GRADUATE FELLOWSHIP PROJECTS PROGRESS REPORTS SPRING 2005

PROJECTS

ALPHABETIZED ACCORDING TO STUDENT LASTNAME

PROJECT NO	STUDENT NAME	PROJECT TITLE	ADVISOR
25	ENIS AKAY	MIMO Physical Layer (PHY) Alternatives for 802.11 Wireless LANs	ENDER AYANOGLU
24	INANC INAN	MAC Algorithms for 802.11 Wireless LANs	ENDER AYANOGLU
4	ARULSAVARANA JEYARAJ	Video Coding and Power Consumption for Mobile Handheld Devices	MAGDA EL ZARKI
2	BYONG-MOO LEE	Adaptive Pre-Distorters for Linearization and Increased Power Efficiency for OFDM-Based Mobile Wireless Communications	RUI DE FIGUEIREDO
15	YUN LONG SUDEEP PASRICHA	SOC Power Optimization Framework	FADI KURDAHI NIKIL DUTT
7	AHMAD YAZDI	Design of Equalizers for High-Speed Wireline Communications Systems	MICHAEL GREEN
9	SHENG-FENG YEN	Analysis of Subtrate and Power/Ground Noise Effects on High-Frequency Mixed Analog/Digital Integrated Circuits	PAYAM HEYDARI

Progress Report on MIMO Research: Spring 2005

Enis Akay, Advisor: Ender Ayanoglu
Center for Pervasive Communications and Computing
Department of Electrical Engineering and Computer Science
The Henry Samueli School of Engineering
University of California, Irvine
Irvine, California 92697-2625
Email: eakay@uci.edu

Achieving high throughput while maintaining robustness is one of the biggest challenges in wireless communications. In general, practical systems sacrifice the crucial diversity that is required for high performance in exchange of higher spatial multiplexing.

It is known that multi-input multi-output (MIMO) systems provide significant capacity increase [1]. MIMO systems also achieve a high diversity order. A technique that provides high diversity and coding gain with the help of channel state information (CSI) at the transmitter is known as beamforming. Beamforming separates the MIMO channel into independent subchannels. Therefore, multiple streams of data can be transmitted easily. Single beamforming (i.e., sending one symbol at a time) was shown to achieve the maximum diversity in space with a substantial coding gain compared to space time codes [2]. If more than one symbol at a time are transmitted, then the technique is called multiple beamforming. For uncoded multiple beamforming systems, it is shown that while the data rate increases, one loses the diversity order with the increasing number of streams used for flat fading channels [3].

Bit interleaved coded modulation (BICM) was introduced as a way to increase the code diversity [4]. In our earlier work, we showed that with the inclusion of BICM to the system, one does not lose the diversity order with multiple beamforming even all the subchannels are used. That is, we showed that multiple beamforming with BICM (BICM-MB) can achieve full diversity order of NM, and full spatial multiplexing of $\min(N, M)$ for flat fading channels using N transmit and M receive antennas. In order to guarantee full diversity, we found a design criterion for the interleaver.

If the channel is frequency selective, then OFDM can be used to combat intersymbol interference (ISI). Hence, by combining BICM-MB with OFDM, one can achieve full spatial multiplexing of $\min(N, M)$ with full spatial and frequency diversity order of NML for L-tap frequency selective channels.

In our previous report, we showed simulation results illustrating gains of 10 - 20 dB when BICM-MB is used.

During Spring quarter, we investigated different power allocation techniques to further improve the performance of our BICM-MB systems. Preliminary results show that instead of providing more power to weaker subchannels, one should allocate more power to better subchannels. This fact arises due to the usage of strong error correcting codes. We are working on an optimization problem to optimally allocate power to each subchannel (and subcarrier if OFDM is used).

Furthermore, we are currently working on designing new codes for BICM-MB. The known convolutional codes do not guarantee full spatial multiplexing and full diversity for different spatial multiplexing, S, values. In our earlier work, we provided a code design criterion to achieve full spatial multiplexing and full diversity for any number of antennas. Our goal is to develop codes that satisfy this code design criterion. We developed and algorithm to do an exhaustive search through possible polynomials that can be used as binary convolutional codes. The polynomials are first checked using "catastrophic code" criteria. If the code is catastrophic, then another set of polynomials are chosen. Once an uncatastrophic code is found, then we look at all-zero path, and all other paths that diverge and converge from all-zero path. When these paths are compared with all-zero path the d_{free} of the code can be found. Comparing the paths also allows us to check whether our design criterion is met. The algorithm runs (by changing the set of polynomials) until the best code (highest d_{free} code) satisfying our design criterion is found. The algorithm is flexible enough to provide any k/n code with constraint length ν.

Some of our findings are available as the draft of a paper we are preparing for publication [5]. We also submitted two journal papers on this topic [6], [7].

REFERENCES

[1] G. Foschini and M. J. Gans, "On limits of wireless communcations in a fading environment when using multiple antennas," *Wireless Personal Communications*, vol. 6, no. 3, pp. 311–335, March 1998.
[2] E. Akay, E. Sengul, and E. Ayanoglu, "Performance analysis of beamforming for MIMO OFDM with BICM," in *IEEE ICC '05*, Seoul, Korea, May 2005.
[3] E. Sengul, E. Akay, and E. Ayanoglu, "Diversity analysis of single and multiple beamforming," in *Proc. IEEE VTC Spring '05*, Stockholm, Sweden, May 2005.
[4] G. Caire, G. Taricco, and E. Biglieri, "Bit-interleaved coded modulation," *IEEE Trans. Inform. Theory*, vol. 44, no. 3, May 1998.
[5] E. Akay, E. Sengul, and E. Ayanoglu, "Achieving full spatial multiplexing and full diversity in broadband wireless systems," *in preparation*.
[6] E. Akay and E. Ayanoglu, "Achieving full frequency and space diversity in wireless systems via BICM, OFDM, STBC and Viterbi decoding," *in review for publication*.
[7] E. Sengul, E. Akay, and E. Ayanoglu, "Diversity analysis of single and multiple beamforming," *in review for publication*.

Designing Efficient Scheduling Algorithms for Variable Bit Rate Traffic in 802.11e WLANs

Inanc Inan (Advisor: Ender Ayanoglu)
Center for Pervasive Communications and Computing, EECS Department
The Henry Samueli School of Engineering, University of California, Irvine
Irvine, California 92697-2625
Email: iinan@uci.edu

I. Introduction

In order to meet negotiated QoS requirements of WLAN traffic, IEEE 802.11e standard document proposes a simple reference scheduling algorithm for HCCA [1]. However, this algorithm can only be efficient for flows with strict Constant Bit Rate (CBR) characteristics. On the other hand, most real time applications for audio and video transmission have Variable Bit Rate (VBR) characteristics.

In Spring'05, we studied designing HCCA scheduling algorithms which can capture VBR characteristics of multimedia traffic.We inserted a number of scheduling algorithms proposed in the literature into our ns-2.28 HCF MAC module [2]. Detecting the shortcomings of those, we are studying a unified scheduling algorithm which combines the strengths of the proposed algorithms and performs adaptively depending on the VBR traffic type.

The contributions of this study are:

- An efficient adaptive HCCA scheduling algorithm for different types of VBR multimedia traffic
  - VoIP with voice activity detection (variable packet interval, constant packet size)
  - MPEG-4 video transmission (constant packet interval, variable packet size)
  - H.261/H.263 video transmission (variable packet interval, variable packet size)
- Appropriate handling of instantaneous traffic conditions using the information available at AP
  - Exact instantaneous downlink traffic knowledge available at transmission buffers
  - Estimated uplink and direct link traffic knowledge
- Efficient use of information obtained from 802.11e MAC header fields of previous frame transmissions in TXOP assignment, e.g. txop requested, more data fields etc.
- Piggybacked frame transmissions in CAP in order to decrease POLL/ACK overhead
- Comprehensive analysis of HCF performance in simulations, i.e. alternating operation of EDCA and HCCA
- A call admission control algorithm for the proposed real-time traffic scheduler

II. HCCA Scheduling

The scheduling algorithm IEEE 802.11e standard [1] has the basic flaw that it always sticks with fixed TXOP values, polling order and interval which do not capture instantaneous traffic conditions of mostly variable bit rate and/or bursty multimedia/internet traffic. FHCF scheme [3] extends the standard's scheduler by using queue length estimations to tune its time allocation to stations, still leaving the polling list and interval static, which sometimes lead to significant transmission delays. Moreover, rather than using queue size information of VBR traffic and making estimations at AP as proposed, stations can calculate exactly the txop requested, and send the result to AP instead.

Grilo [4] uses a variant of Earliest Due Date (EDD) algorithm of real time scheduling theory, Delay-EDD, where deadlines are decided according to delay bounds of the flows. The stations are polled with variable service intervals and HCCA TXOPs are assigned with respect to an aggregate token bucket of aggregate burst size filled at aggregate mean data rate. Varying service interval and TXOPs improve VBR traffic performance, but still the algorithm misses the handling of instantaneous traffic conditions as well as activity detection which may lead significant POLL/NULL overhead decrease for on/off traffic (e.g. VoIP). Neither downlink/uplink traffic are handled separately, nor piggybacking defined in the standard is introduced to the algorithm.

III. Simulation Methodology

The ns-2 simulator with the HCF MAC module [2] is used. At the application layer, traffic is generated using realistic models or real traces. Results from the detailed simulation model show that much better channel utilization and considerably improved performance can be provided. The details of the proposed scheduling algorithm and comprehensive simulation analysis can be found in an upcoming paper [5].

References

[1] IEEE 802.11 WG. Draft Supplement to IEEE Standard 802.11: Medium Access Control (MAC) Quality of Service (QoS) Enhancements, IEEE P802.11e/D11.0, October 2004.

[2] Inanc Inan, 'Design, and Implementation of an IEEE 802.11e HCF Simulation Model in ns-2.27,' CPCC Progress Report, Winter 2004.

[3] Pierre Ansel, Qiang Ni, Thierry Turletti, 'An Efficient Scheduling Scheme for IEEE 802.11e,' Modeling and Optimization in Mobile, Ad-Hoc and Wireless Networks (WiOpt) 2004, March 2004.

[4] Antonio Grilo, Mario Macedo, Mario Nunes, 'A Scheduling Algorithm for QoS Support in IEEE 802.11e Networks,' IEEE Wireless Communications Magazine, June 2003.

[5] Inanc Inan, Feyza Keceli, Ender Ayanoglu 'Providing QoS Guarantees for Variable Bit Rate Traffic in 802.11e WLANs,' in preparation.

Research Progress Report for Spring 2005

Student Name: Arulsaravana Jeyaraj
Advisor/PI: Magda El Zarki

The current focus of our research is in the area of cross layer design for real-time video communications using Multiple Input Multiple Output (MIMO) systems at the physical layer. Our research focuses on cross layer design between the video application layer and the MIMO physical layer. MIMO research has promised enormous increase in capacity for wireless systems. Also MIMO based wireless systems operate under fading conditions typical of wireless channels which face arbitrary quality fluctuations. Since the wireless channel changes over each coherence period, the capacity of the wireless channel, given the power constraints, changes. Hence to make efficient use of the available capacity one needs to adapt the video bit rate. In other words, depending on the capacity, a quality of service could be changed. However it is impossible to adapt at the application layer as the changing parameters of the video takes more time than the coherence period of the channel. Hence by the time the video layer reacts the physical layer faces a new channel. From a different perspective, the physical layer traditionally is assumed to have no knowledge of the video semantics. One solution is to speed up the hardware at the application layer that would enable it to react to the channel status. However, this is impractical and costly.

We propose a novel solution to this problem through the use of layered video using Fine Granular Scalable (FGS) video. A practical solution is to make changes to the video format so that the physical layer does not need to know the video semantics to adapt. Traditionally FGS video quality adjustment is made at the video layer. The FGS format has two layers – the Base Layer (BL) and the Enhancement Layer (EL). It is sufficient to receive the BL for acceptable video viewing. The extra EL bits serve only to increase the video quality enhancing the viewing experience. FGS has a natural ordering at the EL from higher priority bits to lower priority bits. Also it is possible to truncate the EL at any point. This gives the flexibility at the physical layer to discard bits whenever it is deemed necessary as the channel fluctuates in quality. Since the EL can be truncated anywhere knowing the semantics of the video is not necessary at the physical layer. We have designed a cross layer video adaptation system that guarantees the transmission of the BL for a predetermined amount of non-outage periods (for example, 95%). Since the physical layer does not need to know the semantics of the video to adapt, the physical layer truncates bits in real-time. This truncation will for all non-outage periods happen at the EL and not at the BL.

Prior to our research, the only way to handle any change in available capacity would be to drop packets arbitrarily. This, in many cases could be an over kill and there is no way to fine tune quality in real time. The novel design introduced provides enormous flexibility at the physical layer to control video quality and is very practical. We presented proof of concept of the system in a conference paper. The control of video adaptability in real time at the physical layer is being investigated for other possible applications such as multi user video.

Project Name: Adaptive Pre-Distorters for OFDM-Based Mobile Wireless Communications
CPCC Affiliate Professor: Prof. Rui J.P. de Figueiredo
Address, Tel., e-mail; Eng. Tower 616F, Irvine, CA, 92697-2625(949) ; 824-7043; rui@uci.edu
Student: Byung Moo Lee
Date: June 17, 2005

Introduction: To mitigate the Peak-to-Average-Power Ratio (PAPR) in OFDM, which seriously limits the linear range of the High Power Amplifier (HPA), we are developing two different approaches, adaptive digital Pre-Distortion approach and Peak-to-Average Power Ratio management approach.

Summary of Accomplishments: In the Spring Quarter 2005, we completed one conference paper [1] and this paper was accepted in IEEE 7th Emerging Technologies Workshop, St.Petersburg, Russia, June 23 - 24, 2005. And we are preparing two more journal papers [2-3].
In [1], we present a linearization technique of time-varying Solid State Power Amplifier (SSPA) using LMS algorithm. We assume adjustable parameters of SSPA are time-varying with Gaussian distribution and PD tracks the variation of parameters using LMS algorithm. According to the simulation results, our approach is quite promising.
We are ready to send [2] and [3] for publications. In [2], we describe implementation issues of PD for SSPA in detail. In this paper, we provide the design of a tracking algorithm for the case in which the practical HPA is unknown and varying. Simulation results are presented to investigate the performance improvement of the pre-distorter, and to study the distortion effects caused by saturation, overflow, and quantization with different bit-widths, since the bit-width of OFDM base-band (OFDM BB) and DAC/ADC is limited by cost and design constraints in real systems. We are planning to send this paper to the IEEE Transactions on Circuit and System II.
In [3], we present PDs for TWTA and SSPA and compare our PDs with polynomial approximation approach. We assumed that the change of parameters in HPA is Gaussian distribution and tracked the variation of parameters using the LMS algorithm. Even we assume parameters change symbol by symbol, our PDs track well the variation of parameters.
Regarding PAPR reduction technique, in collaboration with Dr. Lin Fang of our Laboratory, we developed a simple new scheme which employs "adaptive input power processing" to reduce the instantaneous power fluctuation of OFDM signals. In so doing we minimize the mean square error between instantaneous power and a target average power using the LMS and RLS algorithms. The present approach avoids the nonlinear distortion in companding at low complexity due to its piecewise linear power adjustment at the receiver. In our scheme, on the transmitter side, the segments of the OFDM signal with high power, are pushed down and the ones with low power are pulled up by adaptive adjustment of input power. As a consequence, the PAPR is greatly mitigated due to the reduction of the range between the peak and lowest power. On the receiver side, the power-adjusted OFDM signals are restored to their original form based on the power adjustment factors that are sent together with the modified signal. Simulation results show that the present scheme requires as low as around 3% bandwidth overhead to transmit the side information of power adjustment factors, and substantially reduces the PAPR by an amount of 1.5~3.5dB depending on the choice of the adaptive algorithm. Besides, the proposed adaptive power scheme is shown to yield better performance with lower bit-error-rate (BER), and also increases HPA power efficiency.

On going work: Even though the PD approach constitutes one of the best solutions for compensation of nonlinear distortion in HPA, the Pre-Distorter technique only works in the limited range of input signal amplitude. As our second approach, we are trying to obtain a solution taking into account signal values beyond the amplifier saturation range. This we call a "Systems Management" approach to Peak-to-Average Power Ratio (PAPR) reduction. In this approach we will pose the underlying problem as an optimization problem and use genetic algorithms for intelligent search of the optimal or suboptimal solutions. More specifically, our aim is to develop low complexity PAPR reduction technique with little bandwidth expansion. We can divide this work as two folds. The first one is to develop a novel PAPR reduction technique based on intelligent search through a genetic algorithm. The second is clipping noise analysis and cancellation using appropriate noise models.

References:

[1] Byung Moo Lee and R. J.P. de Figueiredo, "A Tunable Pre-Distorter for Linearization of Solid State Power Amplifier in Mobile Wireless OFDM" *to appear in IEEE 7th Emerging Technologies Workshop*, St.Petersburg, Russia, June 23 - 24, 2005
[2] R. J.P. de Figueiredo, Lin Fang and Byung Moo Lee, "Hardware Implementation of New Pre-Distorter for SSPA in Wireless OFDM systems" *In preparation for journal publication*.
[3] Byung Moo Lee and R. J.P. de Figueiredo, "Linearization of Time-varying High Power Amplifier using Adaptive Pre-distorters in OFDM Wireless Communications" *In preparation for journal publication*

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

CPCC Fellowship Third Quarter Progress Report, June 2005

Project Name: **SOC Power Optimization Framework**

Graduate Students: **Yun Long**, EECS (on CPCC Fellowship for SQ05)
Sudeep Pasricha, ICS (on CPCC Fellowship for SQ05)

CPCC Affiliate Professors: Fadi J. Kurdahi and Nikil D. Dutt

Project overview

The long term goal of the proposed project is to develop a system level methodology for power optimization for SoCs. In the immediate term, the proposed project will investigate techniques for efficient power modeling of SOC bus architectures, as well as of system-level IP blocks, and their use in the architectural exploration of IP-based SOC designs. On the basis of such power models of the system, we will be able to explore the architectural design space and evaluate various scheduling schemes. Meanwhile, the model is designed to be easily refined as the design process goes through the design flow, giving more accurate estimating of system performance and power consumption. The major purpose of the model is to provide a vehicle for researches on power optimization, such as the HAIM/DOSE (Hierarchically Abstracted IP modeling by Data Organization Space Exploration) exploration flow proposed earlier. The model and exploration flow are based on the COMMEX transaction-level communication architectural framework, on which we will study the H.264 application (the latest video coding standard), and JPEG2000 (the latest still image coding standard).

Progress

During SQ05, we engaged six students in this project and made significant progress. Yun Long and Sudeep Pasricha focused on SystemC modeling framework design. Ishvarjit Garewal and Luis Bathen started modeling H.264 decoder and JPEG2000 encoder in SystemC. Youg-Hwan Park and Luping Zhou progressed well on ASIC design tasks of the same two systems and provided us important implementation data. To conclude, we have achieved the following:

- Finished *Sysplore* v0.1, a SystemC based framework that facilitates SoC system modeling. It hides the communication channel detail and provides unique interface to the functional modules, making it flexible to configure the communication channels and types in a separate configuration file. It aims to ease the transition from the original C code of an application to the SystemC model, which has adequate flexibility to start the following design or modeling refinement flow. *Sysplore* is separated from the original H.264 decoder framework designed in WQ05.
- H.264 decoder modeling on SystemC has started. JPEG2000 modeling has been progressed well, with one of the two most important module finished and the system framework built. System level tiling exploration has been enabled in the framework. Modeling of these two systems will continue through FQ05.
- ASIC design of H.264 decoder is 50% finished. Useful implementation data, including time and power, is being collected for high level modeling. Our future work includes the implementation of the rest of the design and alternative designs for certain modules. The whole implementation work will continue through FQ05. The implementation data of JPEG2000 is also being collected from a VLSI design course project based on an earlier research project. Some finish-up work will be conducted during summer ‘05.

Going forward, our goal is to finish the System model, integrating in the performance and power data acquired from the ASIC design task, and study power optimization techniques with the help of easy design configuration of the model and accurate power modeling. The model will be able to easily and rapidly migrate to any multimedia application systems.

Progress Report Spring 2005
Project: Design Techniques Toward a Full-Rate 40Gb/s Transmitter in 0.18μm CMOS

Introduction: Serial data communication systems are operating at throughputs up to 40Gb/s. Up to now, communications integrated circuits operating at such high speeds have been realized using GaAs, InP, or SiGe bipolar technologies. The design of a 40 GHz voltage-controlled oscillator (VCO) is one the major challenges in the design of a full-rate transmitter. Due to the small inductance needed for resonating at 40 GHz, a regular 40 GHz LC oscillator is not doable in 0.18μm CMOS technology. As a result a 40 GHz differential push-push oscillator has been design for this work.

Achievements during Spring 2005

- Design of the 40GHz Differential push-push VCO: In this design a 20GHz clock signal is generated by a conventional cross-coupled LC VCO. By adding the two differential outputs, the 20GHz fundamental will cancel, leaving only the second harmonic at the output (40GHz). To have a differential 40GHZ output the 20GHz waveforms are in quadrature

- Phase Noise Analysis: The phase noise of the push-push VCO has been analyzed. Since the 40GHz clock is generated from second harmonic of 20GHz clock, the phase noise analysis shows the 40 GHz has 6dB higher phase noise.

- PLL Design: A PLL is being designed. Since the phase noise of the of the 40GHz clock is controlled by the 20Ghz clock, the 20GHz clock is put into the PLL loop. A multi-phase injection dynamic divider is used for dividing the quadrature 20GHz clock.

Future work during Summer 2005

1. Design and model the transmission line using ADS Momentum tool.

2. Layout the frequency synthesizer and run post layout simulations in preparation for fabrication submission.

Substrate Noise Analysis in Nanometer CMOS ICs

Sheng Yen and Payam Heydari
Center for Pervasive Communications and Computing (CPCC)
Department of EECS, University of California, Irvine
Third-Quarter Report to Supporting Companies

This quarter we continued our research on investigating the impact of substrate noise and P/G bounce on two important circuits widely used in mixed-signal integrated circuits, namely phase-locked loops (PLL) and discrete-time delta-sigma modulators. The substrate noise model developed earlier (explained in the second quarter report) has been utilized to study the clock jitter in clock generators incorporating PLLs. The effect of the clock jitter on the performance of the ΔΣ modulator was studied. It is shown through our experimental studies that substrate noise degrades the signal-to-noise ratio of the ΔΣ modulator while the noise shaping does not have any effect on clock jitter induced by substrate noise. To verify the analysis experimentally, a circuit consisting of a second-order ΔΣ modulator, a charge-pump PLL, and forty multistage digital tapered inverters driving 1pF capacitors was designed in a 0.25μm standard CMOS process. Several experiments on the designed circuit demonstrated the high accuracy of the proposed analytical models.

Substrate noise coupling resulting from fluctuations on the on-chip power supply lines and ground wires due to signal switching of output buffers can have excessively large values when multiple output drivers switch simultaneously. Power and ground fluctuations are out of phase, therefore, we introduce a new term for the fluctuations on the P/G lines. The *effective* P/G noise is the algebraic summation of ringings on the power and ground rails. In fact, the effective P/G bounce is the main source of substrate noise, which causes logic and timing failure in the circuits. To reduce the effective P/G bounce, which is a high frequency waveform, on-chip decoupling capacitors have to be placed in close proximity of output buffers. In practice, decoupling capacitors can be placed at any location that is free after floorplanning. On-chip decoupling capacitors across output buffers make the supply fluctuations in phase with the ground fluctuations, and remove high frequency components from supply and ground variations. In the time domain, an on-chip decoupling capacitor smooths out the variations on power supply and ground wires that would have otherwise been spike-like waveforms. In the frequency domain, it shrinks the spectral bandwidth of the variations.

The operation of a discrete-time ΔΣ modulator implemented using the switched-capacitor circuits depends on the complete charging or discharging during each phase of the clock. Therefore, the effects of clock jitter induced by substrate noise on a switched capacitor circuit can be analyzed by examining its effect on the sampling of the input signal and the reconstruction of the output signal. This also implies an important observation, that is, the effects of the clock jitter on a switched-capacitor ΔΣ modulator is independent of the structure or order of the modulator.

Discrete-time ΔΣ modulators are clocked with a monolithic PLL. To analyze the effects of clock jitter induced by substrate noise, it is needed to study the noise impact on the PLL timing jitter. In this section we briefly study the timing jitter induced by substrate noise in closed-loop phase-locked loops.

Due to their desirable features (e.g. not exhibiting any false lock, having a fast acquisition-time, and retaining a zero-phase offset in the lock condition), charge-pump PLLs, shown in Fig. 1, have found widespread use in frequency synthesis and timing recovery applications. The output voltage of the sequential PFD can be expressed as a linear function of the phase difference. The output voltage of the PFD acts like a control voltage for the switched current sources of the charge

pump circuit. Finally, the transfer function of the second-order PLL having a simple RC circuit as the LPF is easily obtained. For the related formulations and derivations. The main focus is thus on charge-pump PLLs, although the analysis is easily extended to any type of phase-locked loop (e.g., the g_m-based PLL). Fig. 1 shows a simplified system block diagram of a charge-pump PLL circuit employed as a clock generator.

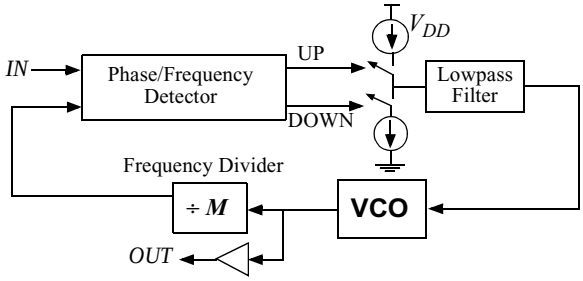

Fig. 1. A system block diagram of the charge-pump PLL

In a PLL-based clock generator circuit, the VCO is the most noise-sensitive circuit among other sub-blocks. The reason is that the VCO is a closed-loop ring oscillator where corrupted zero-crossings of the oscillations due to substrate and supply noise are recirculated in the loop. Moreover, fast jitter components generated by the VCO are not suppressed by the PLL (the PLL operates as a highpass filter to the VCO noise input). On the other hand, the jitter coming from the input terminal does not have much of an effect because firstly, in a PLL-based clock generator the input is coming from a very low-jitter source, and secondly, the PLL loop filter eliminates the in-band components of the input jitter.

The VCO phase noise analysis is carried out by studying a simple conventional differential delay stage commonly used in a ring VCO. To understand the substrate noise effect on the VCO operation, consider a four stage fully differential ring oscillator-based VCO shown in Fig. 2.

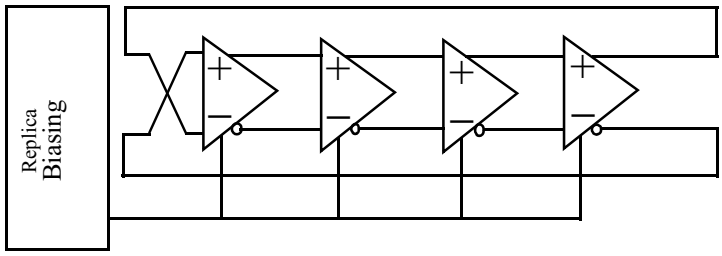

Fig. 2. The VCO based on differential ring oscillator with the voltage controlled resistor and replica biasing.

The VCO incorporates a replica biasing circuitry that always biases the delay element such that the output voltage swing of each differential delay stage is fixed and independent of supply variation. Shown in Fig. 3 is the circuit topology of a differential delay stage being incorporated in the implementation of Fig. 2. The capacitor pair C_D has been employed to neutralize the feed-forward transition provided by C_{GD} of the MOS devices. Each MOS transistor of the differential source-coupled pair experiences a large-signal gate voltage and therefore, it experiences multiple transitions in its region of operation. Moreover, the I_D-V_{GS} relationship of a MOS transistor is nonlinear for both triode and saturation regions. All these phenomena cause the VCO frequency to be a nonlinear function of the supply and input control voltages. This nonlinear relationship is also dependent on the circuit topology being adopted for a delay stage, however, as will be seen later in this section, the general relationship between the excess VCO frequency and substrate

noise remains approximately the same. In most of today's differential ring oscillator architectures the VCO gain is controlled by the tail current which makes it possible to have a wider tuning range and a pseudo-linear frequency-voltage relationship.

The noise propagated through the substrate due to the effective P/G bounce and large-signal switching appear as a common-mode signal for the differential pair transistors, thus does not affect the delay and dynamic operation of the differential pair (*cf.* Fig. 4). On the other hand, substrate noise affects I_{SS} through both the control path and the direct coupling to the tail current's transistor, as shown in Fig. 4. The former component is attenuated by using a differential control input while the latter being almost intact. To capture the short-channel effect of submicron devices, the short-channel MOS model is employed throughout the analysis.

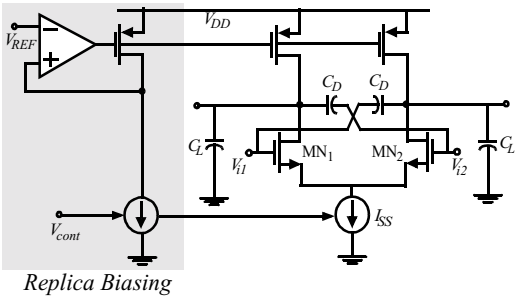

Fig. 3. A simple differential delay stage.

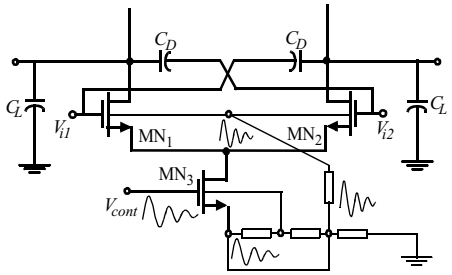

Fig. 4. Substrate injection mechanism for a differential delay stage.

The oscilloscope compares the phase difference between the phase transitions in the clock waveform, separated by an interval ΔT from the reference edge (*cf.* Fig. 5). The oscilloscope, in fact, measures the variance of the zero-crossings.

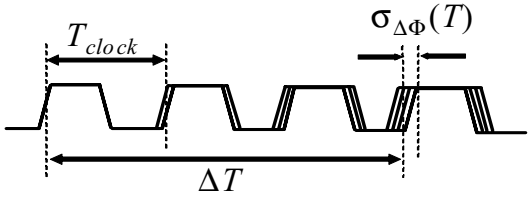

Fig. 5. Definition of the accumulated jitter.

The proposed analytical models are utilized to predict the phase noise and jitter of a PLL-based clock generator due to substrate noise and also to investigate the SNR degradation of the $\Delta\Sigma$ data converter. To verify the proposed analytical models, the following experimental setup is constructed.

To better understand the performance of the ΔΣ modulator in the presence of substrate noise and verify our analytical model, a second-order fully differential ΔΣ modulator with a two-level quantizer is designed in a 0.25μm standard CMOS process. The circuit diagram is shown in Fig. 6.

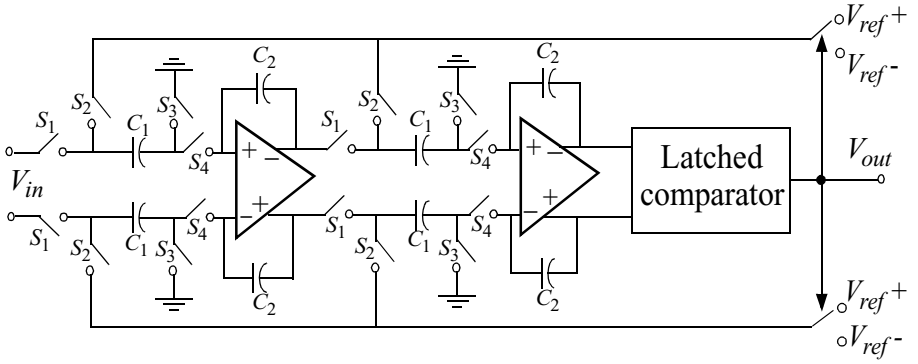

Fig. 6. The circuit diagram of the designed second-order ΔΣ modulator in standard 0.25μm CMOS process

The op-amp used in each delay stage is a simple two-stage fully differential amplifier with a continuous-time common-mode feedback (CMFB) circuit. The latched comparator consists of a PMOS differential pre-amplifier followed by a doubly used PMOS and NMOS cross-coupled regenerative latch. The modulated is operated at the clock rate of 100MHz. The clock to the circuits is provided by a charge-pump PLL circuit. The PLL circuit is also designed in 0.25μm CMOS process with a lock range of 1MHz-500MHz at 2.5V supply voltage.

To experimentally emulate the switchings of digital circuits and to generate the substrate noise caused by logic switching, 40 tapered inverters driving 1pF capacitors are placed around the PLL clock circuit. The circuit is laid out in a low epi process. Post-layout simulations are carried out to account for the metal and interconnect parasitics. To maximally dampen the direct substrate coupling on the sampling network, physical separation is provided between the second-order ΔΣ modulator and the noisy digital circuit. The proposed chip-level substrate network consists of three layers: supply parasitics, the switching transistor circuits, and the resistive mesh modeling the signal propagation in the substrate. The p+ guard ring surrounding the ΔΣ modulator is modeled using a low-resistive network. In an EPI-type substrate technology the injected lateral current from the source of a CMOS circuit (e.g., a CMOS inverter) flows through the heavily doped substrate material because of its low resistivity compared to the inter-layer silicon or epitaxial layer. Moreover, to encompass the randomness of the switching activity of digital circuits, the input signals to the tapered buffers are generated by a pseudo-random generator with a Gaussian distribution. All the circuit simulations are performed using HSPICE. We will investigate the effects of clock jitter induced by substrate noise on the modulator performance.