UNIVERSITY OF CALIFORNIA
IRVINE

CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

GRADUATE FELLOWSHIP PROJECTS PROGRESS REPORTS SPRING 2006

PROJECTS

ALPHABETIZED ACCORDING TO STUDENT LASTNAME

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JUN HO BAHN	Reconfigurable Forward Error Correction Engine	NADER BAGHERZADEH
HAMID ESLAMI	Implementation of Channel Emulator on FPGA	AHMED ELTAWIL
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Progress Report on MIMO Research: Spring 2006

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***Abstract*— In the Spring 2006 quarter we investigated BBO, which is a combination of BICM, single beamforming, and OFDM. We showed that BBO achieves full diversity in space and frequency regardless of the power delay profile (PDP) of the channel. Since only one stream of data is transmitted over all transmit antennas, a simple interleaver is shown to be sufficient to achieve full space and frequency diversity. Simulation results show that beamforming-based systems introduce substantial coding gain, even with partial channel state information at the transmitter (CSIT), when compared to other systems based on space time block codes (STBC) with the same full diversity order. In addition, we show through simulations that reduction of CSIT from full resolution to only one bit per tone results in an SNR reduction of only about 1.5-2 dB.**

I. Introduction

Multi-input multi-output (MIMO) wireless systems allow significant diversity gains for wireless communications. In general, MIMO systems that achieve full spatial diversity with channel state information only at the receiver (CSIR) are known as space-time coding. Some important results of space-time coding systems can be found in [1].

Another technique, which can be used to achieve full spatial diversity over Rayleigh fading channels by utilizing channel state information (CSI) both at the transmitter and the receiver, is known as beamforming. Beamforming separates the MIMO channel into parallel subchannels. When the best subchannel is used, the technique is called single beamforming [2]. If more than one subchannel is used, the technique is called multiple beamforming [2]. In this report we focus on single beamforming, and from now on we will refer to it as beamforming for simplicity.

It is known that a widely used technique, bit interleaved coded modulation (BICM) with orthogonal frequency division multiplexing (OFDM), can achieve the maximum frequency diversity order that is inherited in the channel [3], [4]. We investigated BBO, which is a combination of BICM [5], beamforming, and OFDM. In [6], [7], [8] a more general system transmitting multiple streams of data while maintaining full diversity order was presented. However, BBO presented in this report transmits only one stream of data, and a much simpler interleaver than that of [6], [7], [8] is shown to be sufficient to achieve the full frequency and space diversity independent of the PDP of the channel. In fact, in the simulations of Section II, we used the simple interleaver of the IEEE 802.11a standard. As a result, BBO achieves a diversity order of NML over L-tap frequency selective channels with N transmit and M receive antennas. Simulation results using the IEEE MIMO wireless channel models [9], [10], [11] are also presented in Section II.

For some applications, perfect CSI at the transmitter (CSIT) may not be available. Therefore, we present limited feedback (quantized CSIT) results for beamforming and BBO. We adopted the codebook design approach of [12] and [13], where the codebook is designed using [14]. Only a marginal degradation is observed with limited feedback when compared to perfect CSIT assumption.

II. Simulation Results

Perfect CSIR is assumed for all the simulations below. In order to illustrate partial CSIT for beamforming and BBO, we adopted the codebook design approach of [12] and [13], where the codebook is designed using [14]. The receiver selects the precoding vector that maximizes the effective channel gain and only the index of the codebook is sent back to the transmitter. If b bits per tone are transmitted back, then the cardinality of the codebook per tone is 2^b. For the 2 transmit antenna cases 16 QAM is used for all the systems, and the Alamouti code [15] is deployed for STBC. If the number of transmit antennas is 4, then beamforming systems use QPSK whereas the systems deploying 1/2 rate STBC [1] for 4 antennas use 16 QAM to achieve the same data rate.

Beamforming Results: In this section we present simulation results for 2×1, 2×2 and 4×4 systems. Performance of both beamforming and STBC systems are compared. As shown in Figure 1, both beamforming and STBC achieve diversity order of 2, 4, and 16 for 2×1, 2×2, and 4×4 scenarios, respectively. In addition, beamforming has an 2.5 dB coding gain when compared to the Alamouti code. For the 4×4 case, beamforming provides about 7 dB performance gain when compared to STBC. For the 4×4 case, transmitting back only 2 bits provides more than 5 dB gain compared to STBC, only less than 2 dB loss compared to perfect CSIT.

BBO Results: The BBO system used in the simulations has 64 subcarriers for one OFDM symbol. Each OFDM symbol has a duration of $4\mu s$ of which $0.8\mu s$ is CP. With this setup, channels with rms delay spread of 10 ns and 50 ns correspond to 3 and 11 taps, respectively. The output bits of the encoder

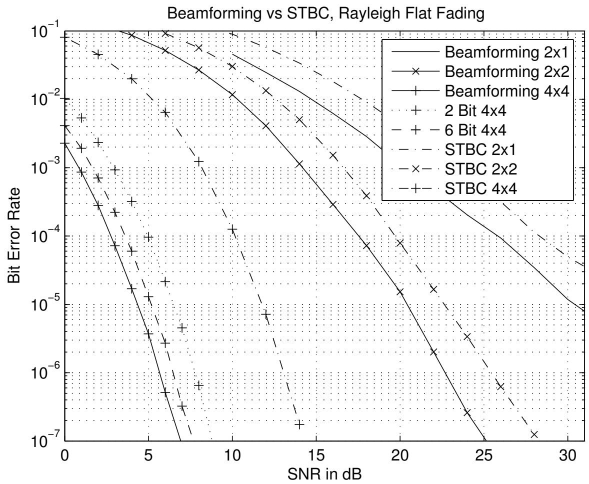

Fig. 1. Beamforming vs STBC results for flat fading channels

are interleaved using the interleaver of IEEE 802.11a [16] within one OFDM symbol. This interleaver satisfies the simple design criterion for BBO.

1) Results using the Equal Power Taps Channel Model: Figure 2 illustrates the results of BBO as compared to a system as a combination of BICM, STBC, and OFDM [4], [17]. Both systems use the same convolutional code with 4 states and $d_{free} = 5$, which is picked from the tables of [18]. As can be seen from the figures, as the delay spread of the channel increases, the diversity order of BBO increases as well. The figures also illustrate that BBO introduces a coding gain when compared to BICM-STBC-OFDM. Although both systems succeed in achieving the same diversity order under the same conditions, BBO shows about 2-3 dB improvement for the 2 transmit antenna case. For the partial CSIT case, even transmitting back 1 bit per subcarrier is shown to provide about 1.3 dB better performance when compared to BICM-STBC-OFDM.

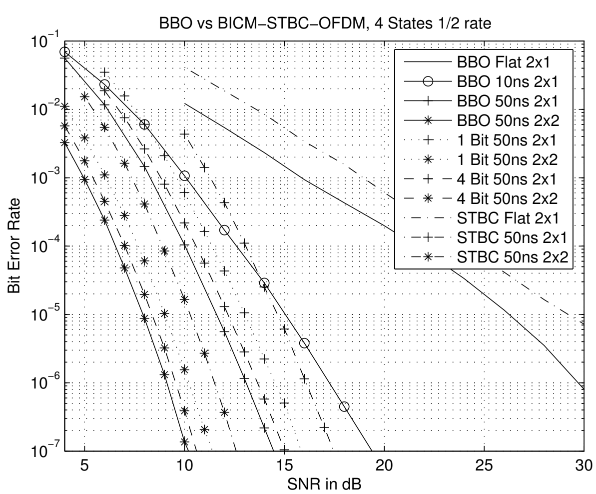

Fig. 2. BBO vs BICM STBC OFDM over different frequency selective channels. 2 transmit 1 receive antennas, 1/2 rate, 4 states $d_{free} = 5$.

Figure 3 presents the simulation results for BBO as compared to BICM-STBC-OFDM when both systems use the industry standard 1/2 rate (133,171) 64 state $d_{free} = 10$ convolutional code. The diversity order of BBO increases with the increasing delay spread of the channel. It can be seen that with increasing transmit and receive antennas, the diversity order of BBO increases as well. As mentioned earlier, BBO introduces a coding gain of 2-3 dB when compared to BICM-STBC-OFDM for two transmit antennas case. The coding gain for the 4×4 case is 6 dB. The partial CSIT case for BBO is also presented, where 2 bit per subcarrier feedback for the 4×4 case is shown to provide about 3.5 dB improvement over BICM-STBC-OFDM.

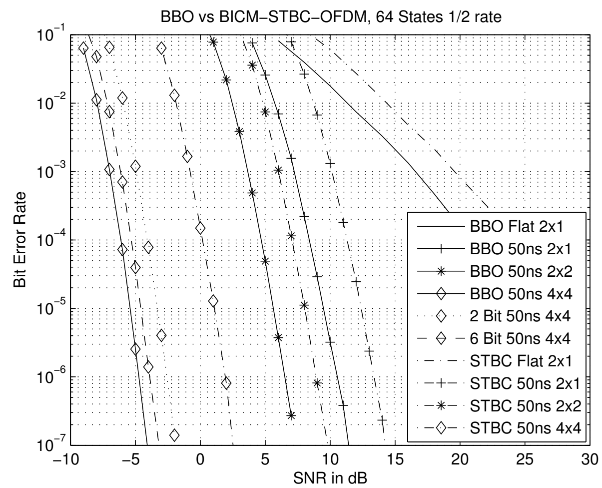

Fig. 3. BBO vs BICM STBC OFDM over different frequency selective channels. 1/2 rate, 64 states, $d_{free} = 10$.

2) Results using the IEEE MIMO Channel Models: Figure 4 illustrates the simulations results using the IEEE channel models [9], [10], [11]. BBO shows 2-3 dB coding gain for the 2×2 case when compared to BICM-STBC-OFDM over IEEE Channel Models B and D. For the partial CSIT case, transmitting 2 bits and 4 bits information per subcarrier back to the transmitter leads to marginal performance loss.

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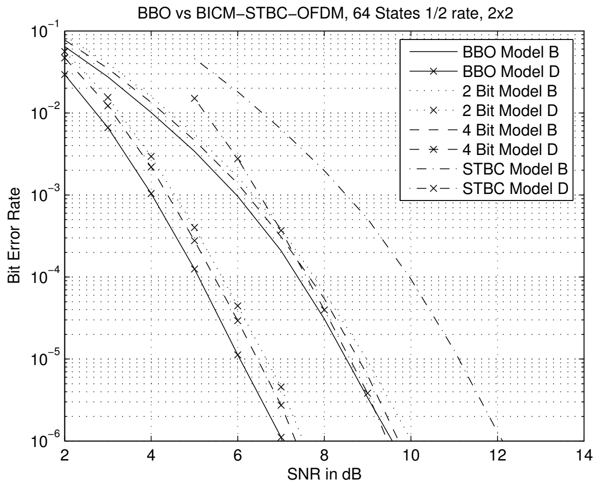

Fig. 4. BBO vs BICM STBC OFDM over IEEE MIMO channel models. 1/2 rate, 64 states, $d_{free} = 10$.

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UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

GRADUATE FELLOWSHIP PROGRESS REPORT SPRING 06

Project Name: Network-on-Chip Architecture in MaRS

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Introduction: In this report, the performance model of a robust Network-on-Chip (NoC) architecture in 2-D mesh topology that uses wormhole routing and a minimal adaptive routing algorithm, is presented. Unlike previous wormhole and adaptive routing models, the model introduced in this report copes with variable node buffer size and message length under the uniform random traffic pattern. The model is validated through comparison with a previous simulation-based model under the same traffic pattern. The contribution of this model is that it provides a simple and accurate model for NoC communication using high-level application. Also it is the first attempt to deal with variable node buffer size and message length in an adaptive routing algorithm.

Summary of Accomplishments: In the Spring Quarter 2006, we formulated an analytical model of Network-on-Chip (NoC) architecture previously proposed. In order to evaluate the performance of interconnection networks, a simulation-based approach is generally used because it is somehow simple. However, this approach is too time-consuming to collect results. As another approach to evaluate the performance, an analytical model of interconnection network is used [1][2].

For our analytical model, certain assumptions are presented as previous models, i.e. arrivals at each incoming port governed by a Poisson process, a uniform random traffic pattern, prioritized contention resolution, immediate consumption of arriving message at destinations, and finally a steady-state network condition. With these assumptions, the whole procedure of building an analytical model is described by following. For the given uniform random traffic and the given dimension of mesh, a steady-state message arrival rate for each port in every node is computed. With the computed steady-state message arrival rate, the blocking probability on each outgoing port is estimated. From the estimated blocking probability, the service time and waiting time at every incoming buffer is derived. Finally by applying the buffer depth and message length variation and averaging latency on every routing path in all possible combination of source and destination pairs, the average latency of interconnection network is calculated. By applying Poisson process assumption, the service time and waiting time is derived from the M/G/1 queuing theory. While validating the model, an interesting relation between buffer depth variation and average latency is found and by applying some adjustment factors on some parameters, the proposed model can be accurate and simple.

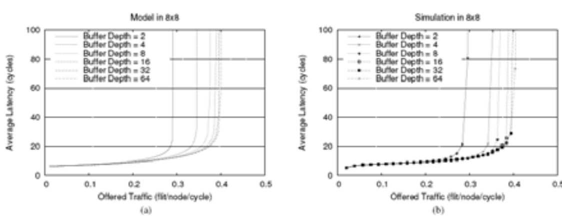

Figure 1. Comparison of average latency in 8x8 with various finite buffer depth

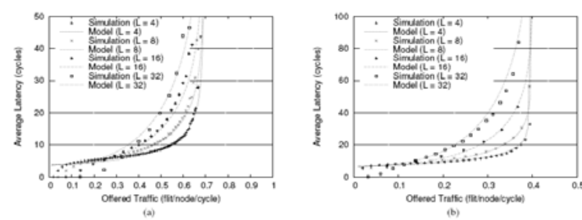

Figure 2. Comparison of average latency in 4x4 and 8x8 with various message length

On going work: Because of increase of hardware complexity for virtual channel, initially the approach to use virtual channels for deadlock freedom was neglected. However, the benefit of virtual channel usage is not only protecting deadlock but also enhancing the maximum throughput [3]. Therefore, by applying this virtual channel concept, an enhanced NoC architecture will be proposed and its performance will be evaluated.

On track of building an enhanced MaRS platform, a timing accurate SystemC™ model of simplified OpenRISC™ core as an EU model will be developed. By merging a SystemC™ router model, finally a SystemC™ MaRS simulator will be constructed which helps faster development of several wireless signal processing components like Turbo and Viterbi algorithms.

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UC IRVINE CENTER FOR PERVASIVE COMMUNICATION AND COMPUTING GRADUATE FELLOWSHIP PROGRESS REPORT Spring 06

Project Name: Ultra High Speed Real-Time Channel Emulation
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Introduction:
Wireless communication system design and implementation are governed mainly by channel models and signal reconstruction algorithms. The time varying nature of the channel leaves the efficiency of such systems highly dependant on the current channel state under which the system is functioning. While statistical models of the wireless channel are sufficient for first order theoretical studies, simulation and experimentation are essential to validate both the theoretical assumptions and results thus leading to a true scientific procedure. Traditional emulation platforms are designed primarily for single input single output systems, where a single wireless channel is assumed to exist between transmit and receive terminals. However with the advent of MIMO based standards such as 802.11n, the need for multi-channel real time emulators is becoming an immediate reality. The challenge in implementing these platforms stems from the fact that the complexity of multi-channel emulators grows quadratically with the number of channels involved. For example, for a 4x4 MIMO system, 16 wireless channels need to be emulated in real time to fully characterize the interaction between all transmit and receive antennas. Furthermore, in highly dispersive environments, each wireless channel by itself can have an extended temporal response which leads to further complexity of the system.
In this research effort, we focus on the design and implementation of a real-time channel emulator for MIMO systems utilizing frequency domain techniques. Adaptive vector-based complex channel emulation in frequency domain algorithms compared to traditional FIR-based emulation results in a drastic reduction in the required computational complexity.

Summary of the Accomplished Work:
This project was partitioned into three phases. In the first phase, wireless channels were studied thoroughly and different wireless channel models were investigated and simulated. Phase one is now complete. The second phase involved designing a system level architecture of the channel emulator that meets the requirements while minimizing the hardware complexity. During this phase, several innovative approaches were introduced to cope with the massive computational load of emulating several simultaneous wideband channels. Namely, an adaptive frequency domain emulation technique was designed and tested. In frequency domain emulation, the frequency representation of the channel is adapted according to the complexity of the pending channel within each coherence time. Since deep fast notches, occur only a small percentage of the time, the frequency representation of the channel can be kept to a minimum for a large percentage of the time, leading to an efficient system. A full discussion of this system including a complexity analysis is presented in a paper entitled, "Ultra High Speed Real-Time Channel Emulation on FPGA" that will be presented at the IEEE Vehicular Technology Conference in Montréal, Fall 2006. A second outcome of this phase was deciding on the optimal partitioning between real-time hardware and non real-time hardware to improve efficiency. Phase two is now complete.
Currently, we are in the final phase, which is the implementation phase, with the target of realizing the designed system on a set of DSP/FPGA boards.

On-going Work: Currently we are working on the implementation of the proposed system model on an FPGA based platform. Reconfigurablity and fast prototyping are the main motivators to choose such a board. A VHDL code to program the hardware platform is under development as the last step to accomplish this project.

Optimal Node Functionality in Memoryless Relay Networks

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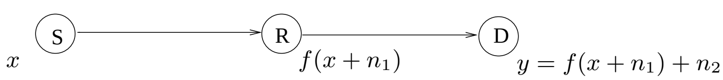
I. Introduction

In a cooperative relay network, the effective channel between the source and destination depends on the signal processing operations performed at the relays. This, in contrast to the traditional design for point-to-point communication, presents us a new challenge in 'designing optimal channel' through optimal relay operation. Our work involves determining optimum relay functionalities for nodes in a relay network.

II. Summary of work

We consider an elementary relay channel as shown below.



Elementary Relay Channel

Relay R observes r, a noisy version of the transmitted symbol x. Based on the observation r, the relay transmits a symbol $f(r)$ which is received at the destination along with its noise n_2.

$$\begin{aligned} r &= x + n_1 \\ y &= f(r) + n_2 \end{aligned} \qquad (1)$$

The relay function f satisfies the average power constraint, *i.e.* $\mathcal{E}_r\left[f(r)|^2\right] = P_R$. We seek to determine the memoryless relay function $f(.)$ that maximizes the following metrics,

- SNR
- Capacity

and compare its performance with existing memoryless forwarding strategies such as amplify and forward (AF), and demodulate and forward (DF).

As the received signal at the destination, y, may have an arbitrary and possibly non-linear dependence on the desired signal x, the SNR definition is not straightforward. To this end, we develop a generalized notion of SNR for the class of memoryless relay functions. The solution to the generalized SNR optimization problem leads to the novel concept of minimum mean square uncorrelated error estimation (MMSUEE). For the elemental case of a single relay, we show that MMSUEE is the SNR-optimal memoryless relay function regardless of the source and relay transmit power, and the modulation scheme. This scheme, that we call estimate and forward (EF), is also shown to be SNR-optimal with PSK modulation in a parallel relay network. The merits of the new forwarding scheme are illustrated in Fig. 1. The results are available in [2] which is under the review process of IEEE JSAC.

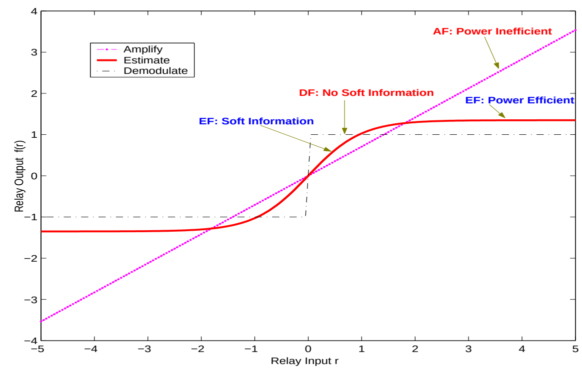


Fig. 1. Relay function of the forwarding schemes

With regard to capacity optimization, we obtain a characterization for the optimal relay function for any modulation scheme at the source. Employing tools of fixed point iteration, we show that the optimal relay function converges to the forwarding strategy of estimate and forward for BPSK modulation. We determine that, with increase in constellation size the relay functions become more and more similar. Ultimately, with Gaussian inputs, the schemes become identical. This can be readily seen as linear MMSE is the unconstrained MMSE for Gaussian inputs. It can also be shown that the MAP demodulation of Gaussian constellation is equivalent to the MMSE estimation. We also consider network topologies with multiple relays such as parallel and serial networks. Consistent with the characteristics of the relay functions from Fig. 1, AF is near optimal in a parallel relay network for its ability to exploit soft information. Similarly, DF is near optimal in a serial relay network as it is power efficient. In both the cases, EF is better than the best of AF and DF. We presented the capacity results [1] at ICC 06, Istanbul.

We are currently exploring relay functionalities for relays with memory so that soft information can be effectively conveyed through network. Our proposed protocol EF when extended to relays with memory outperforms existing schemes for many interesting cases. We are also analyzing scenarios where each node has multiple antennas. The estimate and forward protocol can also be applied in a MIMO relay network where the relay nodes employ distributed space time coding.

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Saturation Throughput Analysis of the 802.11e Enhanced Distributed Coordination Function

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I. Introduction

The EDCA function of IEEE 802.11e standard [1] uses Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA) mechanism as the basic access method. The EDCA defines 4 Access Categories (AC) with AC-specific Contention Window (CW) sizes, Arbitration Interframe Space (AIFS) values, and Transmit Opportunity (TXOP) limits to support MAC-level QoS and prioritization. The outgoing traffic is mapped to an AC according the User Priority (UP) of the corresponding flow.

We have previously designed an accurate Markov model for analytically calculating the EDCA saturation throughput in the assumption of ideal channel conditions for a WLAN scenario comprising 2 ACs [2]. The model accounts not only for AIFS and CW differentiation mechanisms of EDCA, but also for the virtual collision procedure. This quarter, we generalized the proposed model to make it valid and accurate for any number of ACs and arbitrary selection of EDCA parameters. The key contribution is that the proposed Markov chain correctly models the varying number of contending stations thus the varying probability of collision at different AIFS and backoff slots. Comparing the results with the simulation results as well as with the analytical results of state-of-the-art EDCA models, we show that including the correct treatment of such details into the model is vital for the accuracy of theoretical performance analysis [3]. Having exactly matched simulation and theoretical results also verifies the operation of the EDCA function of the HCF module that we have constructed for ns-2 [4], [5].

II. Generalized EDCA Analytical Model

The fundamental performance figure evaluated in this work is the saturation (asymptotic) throughput. The saturation throughput is the limit reached by the system throughput in stable conditions when every station has always backlogged data ready to transmit in its buffer. Although the maximum throughput that can be achieved by the same system can be shown to be higher than the saturation throughput in many scenarios, the operation of a random access scheme at the state of maximum achievable throughput is shown to have unstable behavior [6]. Therefore, the saturation throughput is a practical asymptotic figure analysis of which provides in-depth understanding and insights into the random access schemes and the effects of different contention parameters on the performance.

We model the saturation behavior of each individual AC$_i$ with a different three-dimensional stochastic process $(s_i(t), b_i(t), a_i(t))$ where $s_i(t)$ represents the state of backoff stage, $b_i(t)$ represents the state of backoff counter, and $a_i(t)$ represents the state of AIFS period. With the assumption of independent collision probability at an arbitrary slot, the three-dimensional stochastic process can be represented by a discrete-time Markov chain where (j, k, l) denotes the state of the backoff process of AC$_i$ at time t. We define $0 \leq j \leq r-1$ where r = retry limit, $0 \leq k \leq W_{i,j}$ where $W_{i,j}$ = CW of AC$_i$ at backoff stage j, $0 \leq l \leq A$ where $A = AIFS_0 - AIFS_{i_{max}}$, and $AIFS_0 \geq AIFS_1 \geq ... \geq AIFS_{i_{max}}$. Also, let $p_{b_{i,x}}$ denote the conditional probability that AC$_i$ detects the channel to be busy (there exists at least one transmission) in the current slot given that it has observed the medium idle for $AIFS_x$. Similarly, let $p_{c_{i,x}}$ denote the conditional probability that AC$_i$ experiences either an external or an internal collision given that it has observed the medium idle for $AIFS_x$ and transmits in the current slot (note $AIFS_x \geq AIFS_i$ should hold). Then, the nonzero state transmission probabilities of the proposed Markov model for AC$_i$, denoted as $P_i(j', k', l'|j, k, l)$, are functions of $p_{b_{i,x}}$ and $p_{c_{i,x}}$ [3].

From the steady-state probabilities, $b_i(j, k, l)$, the probability that AC$_i$ transmits at an arbitrary backoff slot, τ_i, can be calculated [3]. The analysis results in τ_i to be a function of $p_{b_{i,x}}$ and $p_{c_{i,x}}$ which are themselves functions of τ_i. This set of non-linear equations can be solved numerically in order to compute τ_i for all ACs.

We are formulating the normalized throughput of a given AC$_i$, S_i, as the fraction of the time occupied by successfully transmitted information. The formulation results in S_i to be a function of τ, which is obtained from the Markov analysis.

III. Numerical and Simulation Results

We validate the accuracy of the numerical results calculated via the proposed EDCA model by comparing them to the simulations results obtained from ns-2 [4], [5]. We investigate the performance for the heterogeneous case when each station has only one single AC active, either AC$_3$ or AC$_1$. We also present normalization throughput prediction of Kong's [7]

TABLE I

CALCULATION AND SIMULATION PARAMETERS

Parameter	**AC$_3$**	**AC$_1$**
$AIFSN$	2	3
CW_{min}	15	31
m	3	
r	7	
Payload Size	1000 bytes	
T_{slot}	9 μs	
$SIFS$	10 μs	

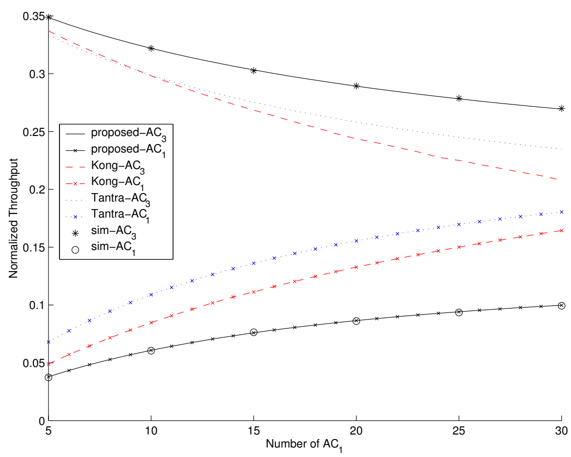

Fig. 1. Analyzed and simulated performance of each AC with a fixed N_3 of 10 and N_1 varied from 5 to 30 for the proposed, Kong's [7] and Tantra's [8] EDCA model

and Tantra's [8] models for the same scenarios. Both in the analytical model and the simulations, the parameters in Table I are adopted. RTS/CTS threshold is set to a small value such that every transmission is assisted with RTS/CTS exchange first.

Fig. 1 shows the normalized throughput performance of each AC with a fixed N_3 of 10 and N_1 varied from 5 to 30. Similarly, Fig. 2 shows the normalized throughput performance of each AC with a fixed N_1 of 10 and N_3 varied from 5 to 30. Fig. 3 displays the normalized throughput performance of each AC when both N_1 and N_3 are varied from 5 to 30 and equal to each other.

The accordance of analysis results with simulation results suggests that our model is highly accurate, and shows no discernable trends toward error for a saturated scenario. We also highlight the importance of exact AIFS and collision probability treatment by comparing the results with EDCA models of [7] and [8].

IV. CONCLUSION

Using the proposed model, the saturation throughput of each AC in a scenario with arbitrary number of ACs having arbitrary AC-specific EDCA parameters can be calculated analytically. The non-existence of a closed-form solution for τ may limit the practical use of the model, but the analysis can effectively assist the EDCA parameter adaptation algorithm or the call admission control algorithm designed for improved QoS support in the WLAN [9].

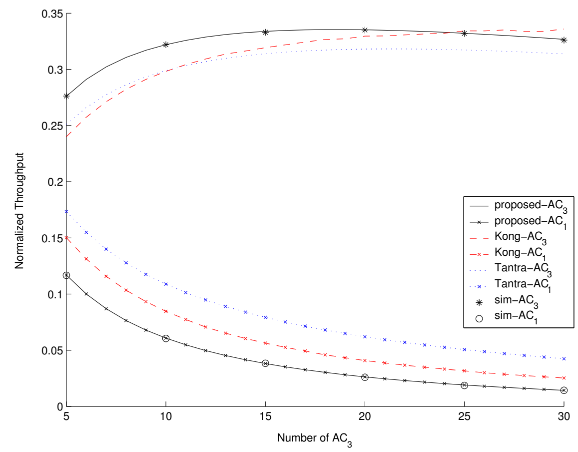

Fig. 2. Analyzed and simulated performance of each AC with a fixed N_1 of 10 and N_3 varied from 5 to 30 for the proposed, Kong's [7] and Tantra's [8] EDCA models

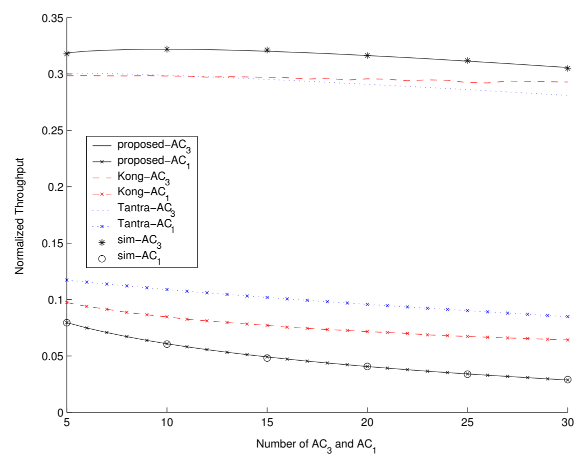

Fig. 3. Analyzed and simulated performance of each AC when both N_1 and N_3 are varied from 5 to 30 and equal to each other for the proposed, Kong's [7] and Tantra's [8] EDCA model

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GRADUATE FELLOWSHIP PROGRESS REPORT

Winter 2006

Project Name: Silicon-based Low-Noise IC Design for Millimeter-Wave Wireless Communication Systems
CPCC Affiliate Professor: Payam Heydari
Address, Tel., e-mail; ET 644C, Irvine, CA, 92697-2625; (949)824-9324; payam@ uci.edu
Student: Vipul Jain
Date: June 27, 2006

Introduction:

The allocation of 7 GHz of unlicensed spectra (22-29 GHz and 57-64 GHz) by FCC has enhanced interest and research aimed at utilizing this resource for high data-rate wireless communication systems such as wireless personal area networks (WPANs), vehicular radars, imaging systems etc. Integrated circuits for these spectra have been implemented in compound semiconductor technologies, but at a prohibitive cost. A CMOS implementation has the capability of bridging the gap between millimeter-wave circuit research and the consumer market.

Summary of Accomplishments:

A significant research effort has been put into the study and design of ultra-wideband K-band RADARs (RAdio Detection And Ranging) in 0.18 micron CMOS technology. This study has led to the design of a homodyne or direct-conversion receiver to be employed in the radar. The front-end consists of a low-noise amplifier, in-phase/quadrature (I/Q) mixers, quadrature voltage-controlled oscillators (VCOs) and a pulse former. The maximum over-all gain of the front-end is 25 dB and the minimum noise figure is 7 dB.

Several existing radar architectures have been investigated in the context of ultra-wideband automotive radar applications. The architecture of choice has been found to be the pulsed radar. A pulsed radar has the advantage of simple implementation which directly reduces the cost and size of the sensor IC of which the radar is a part. Moreover, the pulsed architecture improves the dynamic range of the receiver, directly increasing the range (~30m) of the radar. Other architectures including traditional FM-CW and PN-coded architectures are not suitable to achieve this range.

One of the main limitations in receiver design at these frequencies is the limited gain available from transistors, due to circuit operation close to $f_{max.}$ Moreover, the dimensions of active and passive devices and interconnects become comparable to the wavelengths at these frequencies. Hence, transmission-line effects can not be neglected, and need to be modeled accurately with the aid of 3-D electromagnetic analysis tools. In addition, several test structures including transistors, spiral inductors and transmission lines need to be fabricated and measured in order to characterize their models for these spectra.

In order to solve the above problems, a systematic design approach has been adopted. For accurate passive models, 3-D electromagnetic tools have been employed to determine their frequency response. To characterize the active device models at these high frequencies, test structures have been fabricated in Jazz 0.18 micron CMOS technology. EM-circuit co-simulation techniques have been used to simulate the circuits with EM models in place.

On-going/future work:

The LNA, mixer and LNA+mixer ICs designed in IBM 0.18 micron RFCMOS technology have been received from the foundry, and will be tested during the summer. A 25.5 GHz receiver including the LNA, quadrature mixers, quadrature VCO and a pulse former has been designed and sent for fabrication in June 2006. The chip is expected to be received and tested during the summer. The Ph. D. Qualifying examination was taken and successfully passed on June 20th, 2006. In continuation of the project, design efforts are now being concentrated on the design of the radar transmitter. The ultimate goal is to develop a complete UWB radar transceiver consisting of the receiver and the transmitter on a single chip.

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
GRADUATE FELLOWSHIP PROGRESS REPORT SPRING 06

Project Name: Optimal Routing and Scheduling in Wireless Networks
CPCC Affiliate Professor: Prof. Hamid Jafarkhani
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Student: Javad Kazemitabar
Date: June 28, 2006

Introduction:

Broadband wireless networks today are capable of supporting high data rates. Minimizing the total power in such systems is of paramount importance not just to increase its own operational lifetime in the case of battery powered devices, but also to coexist symbiotically with other systems which share the same frequency spectrum. For instance, 802.11 LANs and Blue-tooth networks share the same unlicensed band and can mutually benefit by limiting the power of their respective signal transmissions.

Summary of Accomplishments:

In the Spring quarter we developed the joint routing-scheduling package for a wireless network. Given the source-destination node pairs and the desired rate among them, our package is capable of both power and route assignment minimizing the total consumed power. Our program is made up of a core MATLAB program assisted with an optimization tool named BARON. In developing this package we studied both the BARON tool as well as the MATLAB interface. In addition, we developed and applied our own optimization algorithms to iteratively find the optimal solution; BARON is only involved in finding the global optimum of a concave function that cannot be handled by MATLAB alone.

On going work:

Previously, optimization algorithms developed for finding the optimal power allocation and routing were unable to work for large networks. In other words, the complexity of their method was exponential in terms of the number of nodes. With our new algorithm, we would like to test our package for large networks. Also, using the benchmark developed, we are planning to approach the general problem of finding the "achievable rates in a wireless network". In the first step, we would like to find inequalities that bound the achievable rates in a given wireless structure.

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[1] R. L. Cruz and Arvind V. Santhanam, "Optimal Routing, Link Scheduling and Power Control in Multi-hop Wireless Networks," Infocom 2003.

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Project Name: Signal Processing for Peak-to-Average Power Ratio (PAPR) Reduction and OBE Mitigation for MIMO-OFDM-Wireless Communication Systems
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Student: Byung Moo Lee
Date: June 10, 2006

Introduction: In Spring 06, we analyzed the performance of the PAPR reduction techniques developed in the Winter Quarter. These techniques are based on a combination of clipping with Selective Mapping (SLM) [1].

Summary of accomplishments: The block diagram of the clipping-with-SLM technique which is used in our combined system is shown in Fig. 1. First, the bit stream is modulated to QPSK/16QAM. Then zero padding is performed when over-sampling is necessary. The SLM block finds the optimum phase set which minimizes PAPR of the OFDM signal. Residual high PAPR signal is clipped by the clipping technique. To reduce spectral leakage, filtering is used when over-sampling is performed.

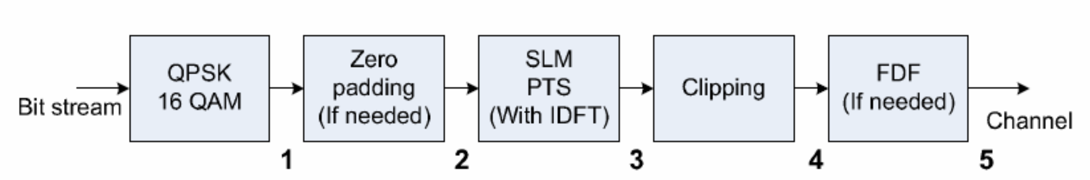

Fig.1. Block diagram of clipping-with-SLM PAPR reduction technique

To develop BER performance analysis of the clipping with SLM technique for fading channels, we used the following two important assumptions which were used in [2]. First, clipping noise is modeled as Additive White Gaussian Noise (AWGN). Second, all of clipping noise falls into in-band. We proved that our theoretical analysis does fit well the simulation results when we use OFDM-QPSK. If we use OFDM-16QAM, our theoretical analysis shows a little bit optimistic results. But both simulation results and theoretical results show similar characteristic.
One more contribution what we got in Spring 2006 quarter is the analysis of clipping at the receiver. Even though we carefully designed the PAPR of the OFDM signal, there are always possibilities that the signal would be clipped at the receiver by A/D converter due to any kind of peak regrowth. Clipping at the receiver shows not so much performance degradation when the channel is flat. However, if the signal is clipped at the receiver when channel is frequency selective, the performance is seriously degraded due to inter-symbol interference (ISI), even though we use enough guard interval.
How much PAPR increases we get, after inserting the guard interval for the SLM PAPR reduced OFDM signal in frequency selective fading channel, has also been analyzed. Basically, if we don't use 100% guard interval, which is usually does not happen in acreal system, guard interval insertion causes peak re-growth even if it is not so severe. This is because we must insert guard interval to the PAPR reduced OFDM signal. Careful consideration after guard interval insertion is necessary to prevent unexpected performance degradation.

On-going work: Obviously, the PAPR problem is not an exceptional case for a MIMO-OFDM system. Since a MIMO-OFDM system has one more dimension (space) compared to SISO-OFDM system, it may also possible to efficiently reduce the PAPR of OFDM signal using the space. We are developing a novel PAPR reduction technique which is especially suitable for MIMO-OFDM systems.

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UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

CPCC Fellowship Spring Quarter Progress Report, June 2006

Project Name: **SOC Power Optimization Framework**
Graduate Student: **Sudeep Pasricha**, ICS (on CPCC Fellowship for SQ 2006)
CPCC Affiliate Professors: **Nikil D. Dutt** and **Fadi J. Kurdahi**

Project overview

The long term goal of the proposed project is to develop a system level methodology for power optimization for SoCs. In the immediate term, the proposed project will investigate techniques for efficient power modeling of SOC bus architectures, as well as of system-level IP blocks, and their use in the architectural exploration of IP-based SOC designs. On the basis of such power models of the system, we will be able to explore the architectural design space and evaluate various scheduling schemes. Meanwhile, the model is designed to be easily refined as the design process goes through the design flow, providing more accurate estimating of system performance and power consumption. The major purpose of the model is to provide a vehicle for researches on power optimization, such as the HAIM/DOSE (Hierarchically Abstracted IP modeling by Data Organization Space Exploration) exploration flow proposed earlier. The model and exploration flow are based on the COMMEX transaction-level communication architectural framework, on which we will study the H.264 application (the latest video coding standard), and JPEG2000 (the latest still image coding standard).

Progress

During Winter 06, we engaged four students in this project and made steady progress. The student supported on CPCC Fellowship was Sudeep Pasricha, who focused on power estimation for on-chip communication architectures, the overall SystemC modeling framework design as well as a case study of the H.264 decoder. Michael Shimasaki finished integration of the RTL design of the H.264 Intra-Prediction module with the AMBA AHB bus. Luis Bathen finished the JPEG2000 encoder modeling in SystemC. Young-Hwan Park worked on gate-level power data extraction for communication architectures, and the H.264 RTL integration effort. During the spring quarter, we accomplished the following:

- Our research focused on creating a system-level power estimation methodology for on-chip communication architectures, specifically the bus matrix communication architecture. We used PrimePower and ModelSim to obtain gate-level power numbers for the bus matrix architecture. Subsequently, we created an energy macro-model methodology using multiple linear regression analysis and used it to create energy models at the system level, for high level power estimation, which is the goal of our SoC Power Estimation Framework. We have found that this methodology is extremely robust and can give us over a 1000X speedup over gate-level estimation. The accuracy of the system-level energy models is within 5% of gate-level power estimates.
- We used the energy macro-model creation methodology to create energy macro-models for the AMBA AHB bus matrix architecture, and used it to perform system-level power-performance trade-off studies. We developed a methodology for power-performance trade-offs in system level synthesis of communication architectures and found that we could get a trade-off space of 20% for power and upto 40% for performance for the application, which is very useful for designers, to select the appropriate solution point from the trade-off graph we generate.
- We are working on integrating the various components of the H.264 decoder at the RTL level with an AMBA AHB-based communication backbone.

Going forward, our goal for the rest of 2006 is to complete the system level power estimation methodology for the communication architectures, as well as other components such as memories, processors and ASIC blocks. We then plan to apply the methodology to study system level power optimization techniques on the H.264 and JPEG2000 application drivers.

Publications

1. Sudeep Pasricha, Nikil Dutt, Eli Bozorgzadeh, Mohamed Ben-Romdhane, "FABSYN: Floorplan-aware Bus Architecture Synthesis", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol 14, No. 3, pp 241-253, March 2006.

Progress Report on MIMO Research: Spring 2006

Ersin Sengul, Advisor: Ender Ayanoglu
Center for Pervasive Communications and Computing, EECS Dept.
The Henry Samueli School of Engineering, University of California, Irvine
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I. INTRODUCTION

We previously showed that the diversity order of uncoded multiple beamforming decreases as more symbols are transmitted simultaneously [1]. We also proved in [2] that if a properly designed bit interleaved coded modulation (BICM) is incorporated to the SVD-based multiple beamforming, one can achieve full spatial multiplexing of $\min(N, M)$ and full spatial diversity of NM for N transmit and M receive antennas over flat fading channels. If the channel is frequency selective, then BICMB is combined with OFDM in order to combat intersymbol interference (ISI) caused by the multipath. The resulting system, named as BICMB-OFDM, achieves full spatial multiplexing of $\min(N, M)$, while maintaining full spatial and frequency diversity of NML for a $N \times M$ system over L-tap frequency selective channels when an appropriate convolutional code is used [3]. Both systems assume perfect channel state information (CSI) both at the transmitter and the receiver.

In indoor environments, transmission schemes are packet-based due to relatively low Doppler spreads and such wireless systems require robust channel estimation to achieve high error performance. Some work has been done to optimized the preamble sequences and structures for OFDM systems [4], [5], [6]. Preamble sequences must have desirable properties in both the time and frequency domains. These include constant envelope properties in the frequency domain, good autocorrelation properties in the frequency and time domain, and low peak-to-average power ratio (PAPR) in the time domain [7].

In practice, perfect CSI may not be available at the transmitter. Furthermore, even the receive side will have imperfect channel estimates especially in the low SNR region. In this study our sole purpose is to analyze the performance of preamble-based channel estimation schemes for previously proposed BICMB-OFDM system. We use the same preamble structure proposed in [8] and compare two different channel estimation schemes considering their corresponding bit-error rate (BER) curves. We analyze the performance degradation BICMB-OFDM [3], which needs channel estimates both at the transmitter and receiver side to perform beamforming. It is assumed that there is an error-free feedback link that conveys the imperfect channel estimates to the transmitter. We also perform simulations for BICM-OFDM-ZF system which does not need CSI at the transmitter side.

One of the two different channel estimation techniques is purely frequency-domain least-squares (LS) estimation (FDE). The other technique of interest is frequency-domain estimation assisted with time-domain windowing with a windowing size of L_0 [9], [10]. If the number of channel taps, L, is known at the receiver, then $L_0 = L$ and the technique is referred as *Joint-known*. If L is not known, then $L_0 = L_{CP}$ which is the worst-case scenario and the technique is called *Joint-unknown*.

II. SIMULATION RESULTS

In the simulations below, the industry standard 64 states 1/2 rate (133,171) $d_{free} = 10$ convolutional code is used. The channel is assumed to be quasi-static and frequency-selective with Rayleigh distribution on each tap. The 802.11n standard has three modes for the preamble [8]. We are interested in the Green Field (high throughput-HT) mode of operation in which legacy 802.11a/g devices are not supported and multiple streams of data are supported. We assume a 2×2 antenna configuration with two streams.

The HT preamble consists of two main parts; one of which is especially designed for AGC, coarse frequency offset estimation and timing synchronization. The second part is designed for channel estimation and fine frequency offset estimation using pilot carriers. We do not use pilot carriers, and we assume perfect frequency offset estimation and timing synchronization. Therefore, we implement the second part of the preamble for each packet transmitted. Note that, cyclically shifted versions of the original preamble are transmitted over multiple antennas simultaneously [8]. We performed simulations with two channel estimation algorithms for BICMB-OFDM and BICM-OFDM-ZF systems.

BICMB-OFDM: BICMB-OFDM system needs to know the channel estimates at both the transmitter and receiver to perform beamforming based on the singular value decomposition (SVD) of the channel in each subcarrier. BICMB-OFDM system outperforms BICM-OFDM-ZF system more than 20dB and the reader is referred to [2] for further details.

Fig. 1-2 show the simulation results for the channel estimation techniques explained in Section I for different delay spreads (6 and 11 taps, respectively). As seen from the figures, in both cases FDE method has a significant performance loss (4-5dB) compared to perfect channel knowledge. However, when FDE is assisted with time-domain windowing and L is known at the receiver the results are 0.5-1dB close to the optimal case. When L is not known, there is further 0.5-1dB performance degradation compared to *Joint-known* case, which makes the estimation of L important.

BICM-OFDM-ZF: Fig. 3-4 show the simulation results for

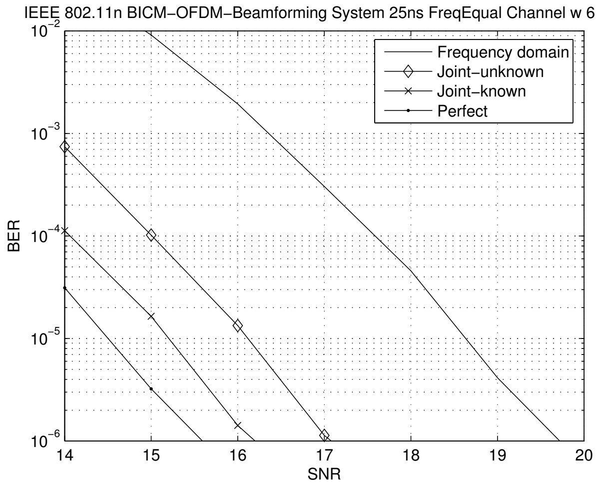

Fig. 1. Results for IEEE 802.11n-Beamforming system over channel with 25ns rms delay spread (6taps).

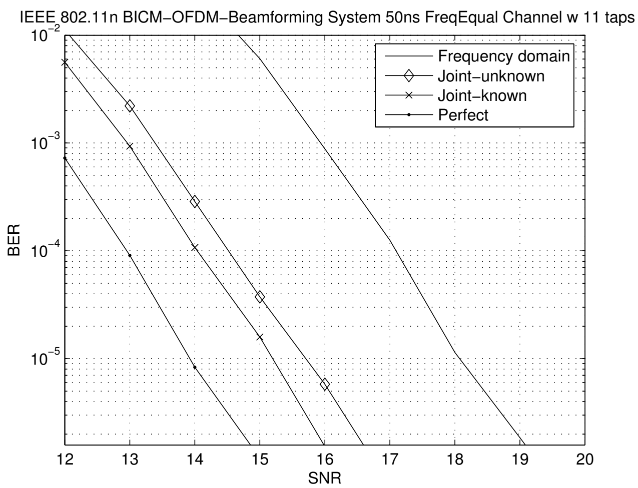

Fig. 2. Results for IEEE 802.11-Beamforming system over channel with 50ns rms delay spread (11taps).

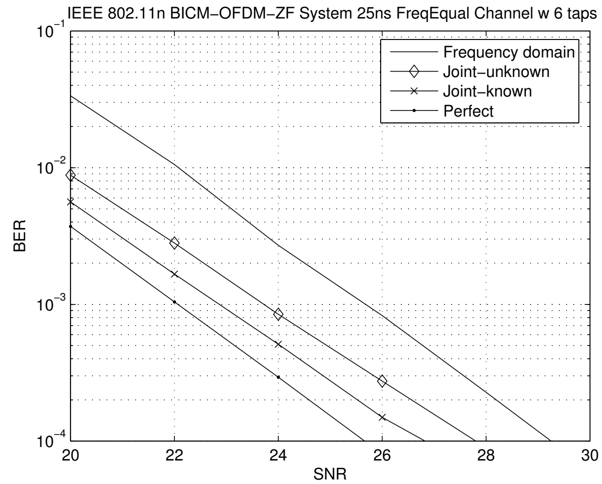

Fig. 3. Results for IEEE 802.11n (with ZF receiver) system over channel with 25ns rms delay spread (6taps).

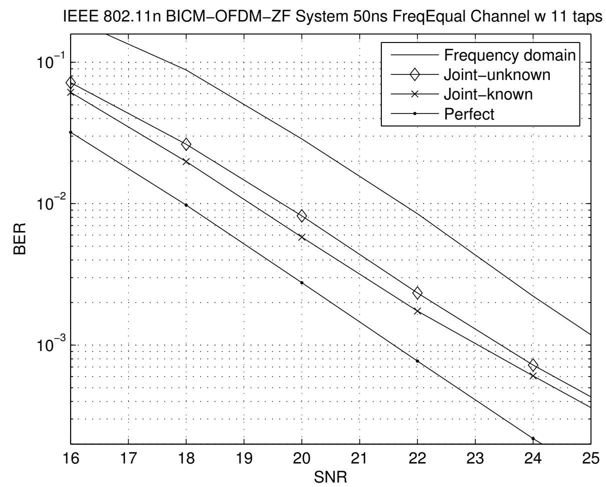

Fig. 4. Results for IEEE 802.11n (with ZF receiver) over channel with 50ns rms delay spread (11taps).

the channel estimation techniques for BICM-OFDM with zero-forcing (ZF) receiver for different delay spreads (6 and 11 taps, respectively). As seen from the figures, in both cases FDE method has a significant performance loss (3.5-4dB) compared to perfect channel knowledge. However, when FDE is assisted with time-domain windowing and L is known at the receiver the results are 1dB close to the optimal case.

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Graduate Fellowship Progress Report (Spring 2006)

Project name:	Cognitive Radio - Opportunistic and Reconfigurable Communication with Distributed Side Information
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Mailing Address:	ET 616E, University of California Irvine, CA, 92697-2625
Phone, E-mail:	(949)824-1684; syed@uci.edu
Student:	Sudhir Srinivasa (sudhirs@uci.edu)
Date:	Wednesday, 28 June 2006

Introduction:

Cognitive radio technology exploits the idea of opportunistic spectrum sharing to improve the utilization of the radio spectrum. A cognitive radio dynamically adapts to spectrum availability by periodically monitoring the radio spectrum, intelligently detecting primary (licensed) user occupancy in the spectrum and then opportunistically communicating over unoccupied channels (spectrum holes) with minimal interference to the primary users. This allows the operation of new wireless devices without the need for any new bandwidth allocation. The cognitive radio environment is dynamic and distributed - the transmitter and receiver have only partial knowledge of the time-varying primary user activity at the other end of the cognitive link. The capacity limits of cognitive radios are fundamental performance measures of these systems in such diverse environments.

Summary of Accomplishments:

Over the past quarter, we have been working on a journal paper [1], to be submitted to the IEEE Transactions on Information Theory.

In [1], we investigate cognitive communication between a secondary transmitter receiver pair over a spectral pool consisting of a finite number of frequency bands (channels). The primary user occupancy processes in the channels are assumed to be independent and identically distributed, and are modeled using Markov chains. The transmitter monitors the radio spectrum for primary user activity and chooses one (if any) unoccupied channel based on a given transmitter policy. Similarly the receiver, based on previously received signals, chooses one of the channels to listen to for secondary transmissions. The receiver and the transmitter have to be matched to the same channel for communication to take place. However, owing to the distributed nature of the primary user spectral activity, the cognitive receiver does not have full knowledge of the channel used at the transmitter for secondary communication. Further, the channel availability changes with time as the primary users dynamically switch on/off. Tracking the transmitter state at the receiver is therefore a primary issue in such channels. We seek to determine the capacity of such a '*tracking*' channel and the corresponding receiver strategy that achieves the capacity. Maximization of the mutual information to obtain the channel capacity involves an intractable optimization over all possible receiver strategies. We instead approach the problem through the notion of '*matching probability*', the probability that the transmitter and receiver are matched to the same channel. We derive a number of genie based upperbounds and training based lower bounds on the matching probability which are then used to obtain tight bounds on the capacity of the tracking channel. We consider different transmitter strategies and analyze the tracking channel capacity for each strategy. With numerical results on the capacity of the cognitive tracking channel, we show that the benefits of spectral pooling disappear in dynamic primary user environments. Further we show that the optimal strategy in such cases is to have the transmitter and receiver hop across frequency bands as dictated by a hopping sequence known to both ends of the link.

On going work:

Simple models for the cognitive radio link have been developed in [1], [2]. We are actively looking at cognitive wireless networks, where cognitive coexistence can be viewed as a perfect middle ground between the extremes of pure competition and pure cooperation. Continuing work includes modeling cognitive multiple access and broadcast scenarios by extending the switch model for cognitive point-to-point links of [1, 2] and also bounding the capacity of such cognitive multi-user wireless networks.

References:

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Project Name: Ultra-Low Power (ULP) Silicon-Based Analog/Mixed-Signal IC Design
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Address, Tel., e-mail; ET 644C, Irvine, CA, 92697-2625; (949)824-9324; payam@uci.edu
Student: Sriramukar Sundararaman
Date: April 12, 2006

Introduction:
Power minimization is one of the most critical objectives in wireless integrated circuit (IC) design. While a rich body of research exists ULP digital IC design, the same cannot be said for analog/RF IC design, partly because the analog/RF ICs, are not amenable to technology scaling. *Unlike ULP digital ICs, ULP RF design is yet to be fully explored.*

Summary of Accomplishments:
We have made a good progress during the THIRD quarter of this project. As we mentioned in the first and the second quarter reports, *the promise of this project is to radically change the way low-power circuits are designed*. Our submitted paper to the IEEE RFIC symposium 2006 was accepted. In addition, we submitted two papers to two IEEE conferences, *IEEE European Solid-State Circuits Conference* (*ESSCIRC*) and *IEEE International Symposium on Low-Power Electronics and Design* (*ISLPED*). Both papers were accepted for oral presentations. Our ISLPED paper was nominated for the **Best Paper Award**.

As stated before, one of the main limitations in the ULP CMOS RFIC design is the low value of transistor's transconductance, g_m, due to the low bias current. In this research, we studied the use of moderately inverted MOS transistors in ultra-low power (ULP) RFIC design. We introduced a new figure of merit for a MOS transistor, i.e., the $g_m f_T$-to-current ratio, ($g_m f_T/I_D$), which accounts for both the unity-gain frequency and current consumption during the optimization process of the transistor's performance. Using this figure of merit while taking into account the velocity saturation of short-channel MOS devices, it was shown both experimentally and analytically that the $g_m f_T/I_D$ reaches its maximum value in moderate inversion region.

In light of the analytical/experimental study presented in our IEEE RFIC symposium paper, a power optimized common-gate low noise amplifier (LNA) operating at 1GHz RF frequency was designed an fabricated in CMOS 0.18µm process. The RF transistor of the power-optimized LNA is biased in the moderate inversion region to maximize the gain-bandwidth product (GBW) for the circuit at the 100µA dc bias current. The RF transistor was biased in moderate inversion region to achieve maximum $g_m f_T/I_D$, which corresponds to achieving the maximum GBW for certain amount of bias current. We just completed measurement of one of the RF amplifiers. The die photo of the circuit occupies an area of 1057µm×865µm. A source follower buffer was placed at the output of the amplifier to avoid the loading effect of the measurement devices at the high impedance output of the LNA circuit. The buffer was also fabricated separately and the final measurement results were derived by de-embedding the effect of the source follower. The de-embedding was achieved by measuring the NF and gain of the buffer separately.

Measurement results show a noise-figure (NF) of 4.9dB and a small signal gain of 15.6dB with a record-breaking power dissipation of only 100µW. The LNA exhibits an IIP3 of -13.7dBm and an input-referred 1-dB compression point of -21.8dBm. The summary of the circuit performance is provided in Table 1.

Table 1: Performance summary of the fabricated common-gate LNA

Parameter	Value
Supply Voltage	1 V
DC Current	100 µA
Operational Frequency	950MHz
S_{11} (dB)	-25 dB
IIP3	-13.7 dBm
P_{-1dB}	-21.8 dBm
Gain	15.6 dB
NF	4.9 dB

On going work:
As a continuation of our project, we will be preparing a journal paper.

Publications out of this Research
[1] Amin Shameli, Payam Heydari, "Ultra-Low Power RFIC Design Using Moderately Inverted MOSFETs: An Analytical/Experimental Study," *IEEE RFIC Symposium,* pp. 521-524, June 2006.

[2] Amin Shameli and Payam Heydari "A Novel Power Optimization Technique for Ultra-Low Power RFICs," to appear in *IEEE Int'l Symposium on Low-Power Electronics and Design* (*ISLPED*), Oct. 2006.

[3] Amin Shameli and Payam Heydari "A Novel Ultra-Low Power (ULP) Low Noise Amplifier using Differential Inductor Feedback" to appear in *IEEE European Solid-State Circuits Conference* (*ESSCIRC*), Sept. 2006.

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING GRADUATE FELLOWSHIP PROGRESS REPORT SPRING 2006

Project Name: Design Techniques Toward a Full-Rate 40Gb/s Transmitter in 0.18μm CMOS
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Introduction: Many bandwidth enhancement techniques have been developed to increase the speed of the CMOS ICs. We combined distributed and lumped techniques to push the technology to the its limit, enabling CMOS technology operating at 40Gb/s. We use the push-push technique to generate a 40GHz clock from the second harmonic of a 20GHz clock. A distributed buffer with 50Ω drain line characteristic impedance and 100Ω gate line characteristic impedance has been designed as the output driver.

Summary of Accomplishments:

Top level simulations have been finished. The coplanar waveguide strip (CPS) for the push-push VCO has been designed with the ADS Momentum 2.5D simulation tool. Two output distributed buffers have been designed with both *LC* lumped transmission lines and CPS lines in order to compare the performance. We decided to use the lumped distributed buffers due to their higher area efficiency. Differential inductors have been designed for distributed buffer to save even more area.

Ongoing Work:

1. Layout & Post Layout Simulation: Post layout simulation includes RCX extraction and EM verification for high frequency blocks. Interconnects in the 20GHz and 40GHz blocks are being extracted with momentum simulation tool.
2. Inductor model is being verified up to the 40GHz by 3D HFSS EM simulator and IE3D.