UNIVERSITY OF CALIFORNIA
IRVINE

CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

GRADUATE FELLOWSHIP PROJECTS PROGRESS REPORTS WINTER 2006

PROJECTS

ALPHABETIZED ACCORDING TO STUDENT LASTNAME

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JUN HO BAHN	Reconfigurable Forward Error Correction Engine	NADER BAGHERZADEH
HAMID ESLAMI	Implementation of Channel Emulator on FPGA	AHMED ELTAWIL
KRISHNA SRIKANTH GOMADAM	Adaptive Partially Coherent Multiuser MIMO Transceiver Design for Rapidly Time Varying Channels	SYED A. JAFAR
INANC INAN	MAC Algorithms for 802.11 Wireless LANs	ENDER AYANOGLU
VIPUL JAIN	Silicon-Based Low-Noise IC Design for Millimeter-Wave Wireless Communications Systems	PAYAM HEYDARI
SEYED JAVAD KAZEMITABAR	Cooperation in a Large Network	HAMID JAFARKHANI
BYONG-MOO LEE	Signal Processing for Peak-to-Average Power Ratio (PAPR) Reduction and OBE Mitigation for MIMO-MC-CDMA Wireless Communication Systems	RUI DE FIGUEIREDO
SUDEEP PASRICHA	SOC Power Optimization Framework	NIKIL DUTT FADI KURDAHI
ERSIN SENGUL	Adaptive Modulation and Coding for Bit-Interleaved MIMO-OFDM Systems	ENDER AYANOGLU
SUDHIR SRINIVASA	Cognitive Radio – Opportunistic and Reconfigurable Communication with Distributed Side Information	SYED A. JAFAR
SUNDARAMAN SRIRAMKUMAR	Ultra Low Power (ULP) Silicon-Based Analog/Mixed Signal IC Design	PAYAM HEYDARI
AHMAD YAZDI	Design Techniques Toward a Full-Rate 40 Gb/s Transmitter in 0.18 μs	MICHAEL GREEN

Progress Report on MIMO Research: Winter 2006

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***Abstract*— Orthogonal frequency division multiplexing (OFDM) is known as an efficient technique to combat frequency selective channels. In our earlier work, we showed that the combination of bit interleaved coded modulation (BICM) and OFDM achieves the full frequency diversity offered by a frequency selective channel with equal power delay profile conditioned on the minimum Hamming distance, d_{free}, of the convolutional code. In Winter 2006, we were able to extend this result to frequency selective channels with any kind of power delay profile. This system has a simple Viterbi decoder with a modified metric.**

I. Introduction

In Winter 2006 quarter, we revisited our earlier work on BICM-OFDM, which can achieve the maximum frequency diversity order available in the channel. Earlier, we showed both analytically and via simulations that the maximum diversity is achieved for frequency selective channels with equal power delay profile (PDP). During Winter 2006 quarter, we were able to extend our results for frequency selective channels with any kind of PDP by using Ostrowski's theorem [1]. Our proof on the diversity order of BICM-OFDM do not require large delay spread and ideal interleaving assumptions. We present an easy to implement design criterion for the bit interleaver to achieve the maximum frequency diversity. BICM-OFDM does not require a priori knowledge of the delay spread of the channel to design the code. If that kind of knowledge is present and the minimum Hamming distance of the convolutional code is larger than the number of taps in the channel, then puncturing can be used to increase the data rate while still achieving the maximum frequency diversity. Or, a higher rate, lower minimum Hamming distance best known convolutional code can be used to achieve the maximum diversity and a higher coding gain compared to the punctured code.

We provide simulation results supporting our analysis in Section II. We made revisions on our previously submitted work. The revised version is currently under review [2].

II. Simulation Results

In the simulations of this section, 64 subcarriers are used for each OFDM symbol. One symbol has a duration of 4 μs of which 0.8 μs is CP. 1000 bytes of information bits are sent with each packet and the channel is assumed to be the same through the transmission of one packet. Coded bits are interleaved with the interleaver given in [3], and modulated onto symbols using 16 QAM with Gray labeling.

Figures 1 and 2 show the simulation results for different rms delay spread values of the frequency selective channel with equal power taps with 64-states and 4-states convolutional encoders, respectively. As can be seen from Figure 1, as the number of taps of the channel increases, the diversity order of BICM-OFDM increases as well to the maximum value of 10. Another interesting observation is that while diversity order for 50 ns and 75 ns channels reach the maximum value, 75 ns channel shows a slightly better coding gain.

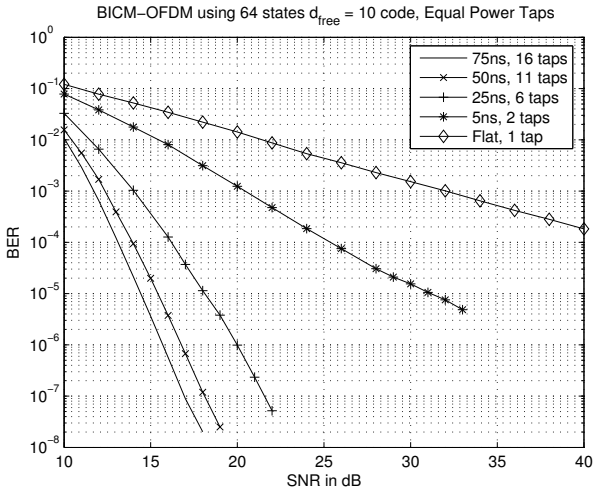

Fig. 1. BICM-OFDM results using 1/2 rate 64 states $d_{free} = 10$ convolutional encoder

From Figure 2, it is clearly evident that as the number of taps for the channel increases, the diversity order increases as well. It can be seen that the maximum diversity order that can be achieved by $d_{free} = 5$ BICM-OFDM is 5. Similar to the results shown in Figure 1, while diversity for 40 ns, 50 ns, and 75 ns channels reach the maximum value (i.e., all the curves have the same slope for high SNR values), 75 ns channel shows a slightly better coding gain.

Figure 3 illustrates the results of BICM-OFDM over equal power taps, and taps with exponential PDP. As can be seen, BICM-OFDM achieves full frequency diversity for different kinds of PDP at asymptotically high SNR values.

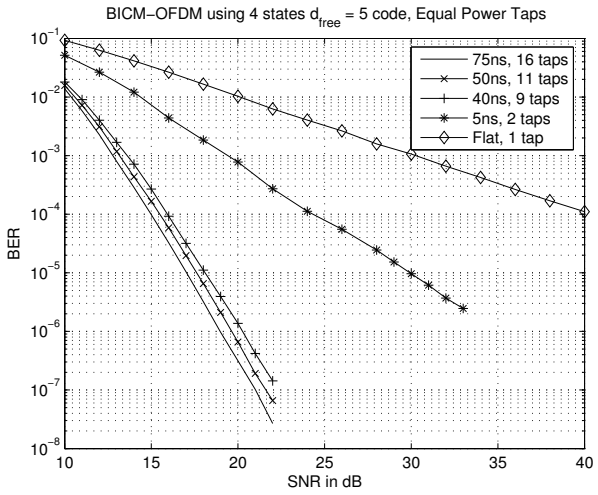

Fig. 2. BICM-OFDM results using 1/2 rate 4 states $d_{free} = 5$ convolutional encoder

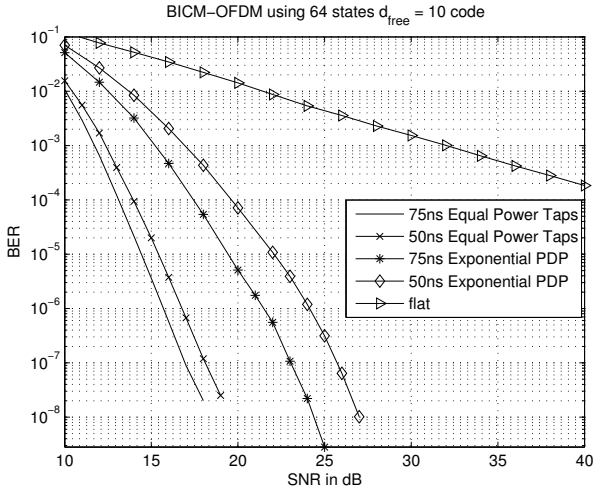

Fig. 3. BICM-OFDM results using 1/2 rate 64 states $d_{free} = 10$ code over equal power taps, and taps with exponential PDP

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UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

GRADUATE FELLOWSHIP PROGRESS REPORT WINTER 06

Project Name: Network-on-Chip Architecture in MaRS
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Date: April 10, 2006

Introduction: In this report, we present several enhanced network facilities which are appropriate for VLSI implementation and have a reduced complexity, high throughput, and simple routing algorithms even if basic network problems such as deadlock and livelock, are considered. We develop a new packet definition to support such different requirement in a MIMD message passing architecture and also verify its efficiency by comparing simulation results. By providing a uniform way of constructing such network architecture, its scalability can be easily accomplished. And this network architecture can be applied to different SoC developments including our MaRS.
The major contribution of this report is the design of Network-on-Chip (NoC) architecture adopting a minimal adaptive routing algorithm with near-optimal performance, feasible design complexity and minimal number of network hops for 2D-mesh networks, thus satisfying all the stated design goals. The proposed adaptive routing algorithm and NoC architecture offer nearly optimal performance which can be shown by comparing O1TURN [1], near-optimal worst-case throughput routing algorithm for 2D-mesh networks.

Summary of Accomplishments: In the Winter Quarter 2006, we refined some specification of Network-on-Chp (NoC) architecture in MaRS such as data formats, routing algorithms, router architectures, etc. and collected additional simulation results for performance evaluation. And using TSMC™ 90nm process technology, our prototype router and FIFO were synthesized again. It shows very competitive design architecture with respect to performance, area, and power. With comparison to the previous synthesized result in TSMC™ 0.18µm process technology, its operating clock is enormously increased to be over 400MHz while at 0.18µm technology it is about 135MHz. The detailed synthesis result is shown in Table 1. Based on the above results, we submitted two papers [2][3] and are preparing one more paper focusing on design implementation of router architecture.

Table 1. Comparison of physical implementation in different process technology

process	TSMC™ 0.18µm process technology		TSMC™ 90nm process technology	
	Router	FIFO (depth = 4)	Router	FIFO (depth = 4)
Operating Voltage	1.8 V	1.8 V	1.0 V	1.0 V
Operating Frequency	135 MHz	325 MHz	423 MHz	1.8 GHz
Area	157,515 µm2	73,580 µm2	11,492 µm2	8,384 µm2
Dynamic Power	27.1410 mW	19.9458 mW	2.2894 mW	5.3338 mW
Leakage Power	267.39 nW	121.70 nW	127.97 nW	77.26 nW

As the other part of MaRS enhancement, we are changing the execution units (EUs) using OpenRISC™ core, which is one of core components in MaRS together with a router. At the initial step for changing EUs, the allocated redundant blocks in the provided OpenRISC™ environment like MMU, I-/D-caches, and other redundant peripherals should be removed to be dedicated in MaRS. With simplified OpenRISC™ RTL codes, we completed basic functional verification.

On going work: For the proposed NoC architecture, a theoretical analysis will be required to provide a simple but accurate abstraction of the router or communication model to higher-level applications such as performance estimator for MaRS. Though many analytical models for deterministic routing algorithms were proposed [4], ones for adaptive routing algorithms [5] like ours are very few and inaccurate because of simplification with lots of assumptions to reduce the analysis complexity. Therefore, it is very challenging to invent an accurate model of NoC architecture. On the other hand, some additional features are being considered for the proposed NoC architecture to be fault tolerant and general. Some facilities supporting power management, EU/PE synchronization, fault tolerance in routing algorithm will be concerned.
On track of building an enhanced MaRS platform, a timing accurate SystemC™ model of simplified OpenRISC™ core as an EU model will be developed. By merging a SystemC™ router model, finally a SystemC™ MaRS simulator will be constructed which helps faster development of several wireless signal processing components like Turbo and Viterbi algorithms.

Reference:

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University of California Irvine
Center for Pervasive Communications and Computing
Winter Quarter CPCC Fellowship Progress Report

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Advisor: Ahmed Eltawil

Previous Work:
In order to emulate dispersive high capacity channels a frequency-domain emulation algorithm was proposed as an alternative for the conventional time-domain algorithms. A comprehensive complexity analysis was performed illustrating a considerable improvement for an 802.11n channel model as the case study. This model benefits from vector-based calculation and adaptive system configurations thank to frequency-domain exploitations. The contributions were presented in a paper submitted to Vehicular Technology Conference, Fall 2006 [1].

Winter Quarter Progress:
In previous work, the algorithm was simulated and evaluated at the system level. Currently, the data-flow of the emulator core is being designed. The core comprises three separate blocks; N-point FFT, multiplier and M-point IFFT where N and M are chosen based on the input and output resolution profiles. To further improve the performance of the system and adaptive mode is investigated where the frequency resolution is a function of the channel impulse response (CIR). N and M are subsequently chosen by the host processor and downloaded on the real-time hardware as an overhead to the CIR. The three modules communicate asynchronously while internally functioning synchronously. Handshaking signals have been designed to control the flow of data between modules (asynchronously). Every coherence time a new set of CIR is downloaded onto the multiplier and its adaptive specifications are downloaded onto FFT and IFFT engines accordingly. Two extra memories where manipulated in the system to eliminate the delays associated with system update. A five-bit register is also allocated in the system by which the processor (a local PC) communicates with the modules.
To maintain high resolution yet minimum work load on the real-time path a thorough fixed point analysis was performed based on the 802.11n channel profile to specify the required width of calculations in each block.

Current Task:
After an inclusive system and hardware level analysis the final system is ready to be implemented. Implementation will be performed using an FPGA platform.

References:
[1] Hamid Eslami, Ahmed M. Eltawil “A Real-Time Wireless Channel Emulator for MIMO Systems” submitted in VTC Fall 2006.

UC Irvine Center for Pervasive Communications and Computing
Graduate Fellowship Progress Report Winter 05

Project: Modulation and Detection for Simple Receivers in Rapidly Time Varying Channels.
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Date: April 12, 2006

Introduction: In the previous report, we highlighted the issues related to channel uncertainty caused by mobility and proposed techniques to exploit partial channel knowledge. We presented the paper [1] at WCNC 06, Las Vegas. The main contributions of the paper are the partially coherent detectors for FSK and DPSK, and the partial CSI based adaptive schemes: intra-block and inter-block adaptation.

We also analyzed how mobility affects different nodes in a cooperative setting. We determined that, despite the symmetry, mobility of source affects the performance much more than the mobility of destination in a coherent cooperative system. We also proposed partially coherent detection and combining strategies at the relay and the destination for amplify-and-forward and demodulate-and-forward-relays. We presented this paper [2] at WCNC 06.

Summary of Work

It can be recalled that the partially coherent detector is a linear combination of coherent and noncoherent detectors with the weights determined by the channel correlation and SNR. As per the reviewers' feedback in [3], we analyze the performance of the partially coherent detector when there is an uncertainty in the knowledge of the channel correlation parameter. In the partially coherent detector, coherent detection gets emphasized when the channel correlation is more and vice versa. Therefore an inaccurate channel statistic results in increased or decreased weights for both the coherent and noncoherent detection. We show that the performance degradation due to inaccurate weights is insignificant for all practical scenarios .We study the two cases where the estimated correlation value is either greater or less than the actual channel correlation. We bound the error probability for both the cases and demonstrate that the partially coherent detector still obtains substantial gain over the best of coherent and noncoherent detection. In order to avoid explicit estimation of the channel correlation, we propose a partially coherent detection scheme that utilizes the minimum possible correlation value as the actual channel correlation. A combination of analytical and simulation results are provided to substantiate the merits of the scheme. We determine that the partially coherent detector achieves a gain of about 2 dB even with inaccurate channel statistics. We have revised the paper [3] incorporating the above mentioned work. We have also included a capacity analysis of modulation schemes in rapidly time varying channels.

In a relay network scenario, we have shown in [2] that significant performance gain can be obtained over conventional detection methods in rapidly time varying channels. A longer version of [2] with a comprehensive analysis on mobility and its effect on detection methods in a cooperative network is under preparation [4]. We also develop a general framework for partially coherent detection for amplify-and-forward and demodulate-and-forward relaying. This framework will be highly useful for detection and combining in a relay network for more than one relay. Future work will include determining optimal weights for a single/multi-user system equipped with multiple antennas. We are also exploring optimum memoryless relay functionalities for a general relay network.

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Performance Analysis of the IEEE 802.11e Enhanced Distributed Coordination Function

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I. Introduction

The IEEE 802.11e standard defines the Hybrid Coordination Function (HCF) which specifies the QoS algorithms in the MAC layer of the next generation 802.11 wireless LAN (WLAN) [1]. The HCF is composed of two access functions: A distributed contention-based channel access function (EDCA) providing prioritized QoS and a centralized polling based channel access function (HCCA) providing parameterized QoS.

Although the EDCA function may provide satisfactory service differentiation in low-load environments, its contention-based nature results in impaired performance, low channel efficiency and lack of QoS guarantee in the presence of heavy traffic load when no call admission control (CAC) is employed. Therefore, in-depth understanding of the EDCA mechanism at the saturated scenario may help to achieve a more successful embedding of QoS-aware 802.11e EDCA function in network schemes as well as to develop efficient CAC algorithms.

This quarter, we have designed a simple EDCA function analytical model which includes contention window and Arbitration Inter Frame Space (AIFS) differentiation and virtual collision scheme for different Access Categories (AC). With results from the ns-2 MAC module we have constructed for 802.11e simulation, we have shown that our model predicts the EDCA saturation throughput more accurately when compared with the models proposed in the literature.

II. Analytical EDCA Model

Throughput and delay analysis of Carrier Sense Multiple Access (CSMA) and its variations has long been a research focus in packet networks. Accompanying the standardization and rapid deployment of IEEE 802.11 WLANs, the performance analysis of its contention-based Distributed Coordination Function (DCF) [2], a CSMA with collision avoidance (CSMA/CA) scheme with slotted binary exponential backoff (BEB), has been studied extensively by analytical and numerical means in recent years. A simple Markov Chain to model the behavior of DCF is proposed in [3]. The model accounts for all the exponential backoff protocol details and allows to compute the saturation (asymptotic) throughput performance of DCF. The key approximation that enables the model is the assumption of constant and independent collision probability of a packet transmitted by each station, regardless of the number of transmissions already suffered. As proven by comparison with simulation, this assumption leads to accurate results, especially when the number of stations in the wireless LAN is large (say greater than five).

Each AC queue in the system is modeled by a Markov process specific to the AC associated with the queue. Our model relies on three discrete time processes to model the progress of a given AC through backoff for a saturated scenario under ideal channel conditions as a three dimensional Markov chain. One process $b(t)$ represents the backoff counter of the station. Since the value of $b(t)$ after transmissions depends on the size of the contention window from which it is drawn , $b(t)$ depends on station's transmission history, and is therefore non-Markovian. To overcome this, [3] defines another process, $s(t)$, to track the size of the contention window (W_i, $i = s(t)$). We are including the third process, $a(t)$, which models the state of the corresponding AC during the AIFS period. The main contribution of the study is that the transition probabilities in $a(t)$ accounts for the AIFS differentiation between different priority ACs. It models the case where higher priority ACs enjoy a lower average probability of collision, since these ACs may transmit in backoff slots that lower priority stations still waiting in AIFS cannot. The model also includes virtual collision scheme defined in [1]. The details on the development of EDCA Markov Model and saturation throughput analysis using this model can be found in an upcoming paper [4]. The steady-state solution for the proposed Markov model results in a set of non-linear equations, so throughput analysis can be carried out via numerical methods. Practical use of this theoretical model is also limited by its restriction to the saturation conditions. On the other hand, it provides additional insights and understanding for the behavior of the EDCA mechanism and may as well guide for efficient CAC algorithm design.

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UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
GRADUATE FELLOWSHIP PROGRESS REPORT
Winter 2006

Project Name: Silicon-based Low-Noise IC Design for Millimeter-Wave Wireless Communication Systems
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Introduction:

The allocation of 7 GHz of unlicensed spectra (22-29 GHz and 57-64 GHz) by FCC has enhanced interest and research aimed at utilizing this resource for high data-rate wireless communication systems such as wireless personal area networks (WPANs), vehicular radars, imaging systems etc. Integrated circuits for these spectra have been implemented in compound semiconductor technologies, but at a prohibitive cost. A CMOS implementation has the capability of bridging the gap between millimeter-wave circuits research and the consumer market.

Summary of Accomplishments:

A significant research effort has been put into the study and design of ultra-wideband K-band RADARs (RAdio Detection And Ranging) in 0.18 micron CMOS technology. This study has led to the design of a homodyne or direct-conversion receiver to be employed in the radar. The front-end consists of a low-noise amplifier, in-phase/quadrature (I/Q) mixers and a frequency synthesizer. The maximum over-all gain of the front-end is 22 dB and the minimum noise figure is 7 dB.

Several existing radar architectures have been investigated in the context of ultra-wideband automotive radar applications. The architecture of choice has been found to be the pulsed radar. A pulsed radar has the advantage of simple implementation which directly reduces the cost and size of the sensor IC of which the radar is a part. Moreover, the pulsed architecture improves the dynamic range of the receiver, directly increasing the range (~30m) of the radar. Other architectures including traditional FM-CW and PN-coded architectures are not suitable to achieve this range.

One of the main limitations in receiver design at these frequencies is the limited gain available from transistors, due to circuit operation close to $f_{max.}$ Moreover, the dimensions of active and passive devices and interconnects become comparable to the wavelengths at these frequencies. Hence, transmission-line effects can not be neglected, and need to be modeled accurately with the aid of 3-D electromagnetic analysis tools. In addition, several test structures including transistors, spiral inductors and transmission lines need to be fabricated and measured in order to characterize their models for these spectra.

In order to solve the above problems, a systematic design approach has been adopted. For accurate passive models, 3-D electromagnetic tools have been employed to determine their frequency response. To characterize the active device models at these high frequencies, test structures have been fabricated in 0.18 micron CMOS technology. A EM-circuit co-simulation technique has been used to simulate the circuits with EM models in place.

On-going/future work:

The LNA, mixer and LNA+mixer ICs designed in 0.18 micron RFCMOS technology have been received from the foundry, and will be tested in the near future. A 25.5 GHz frequency synthesizer has been designed and will be sent for fabrication in May 2006. A complete 22-29 GHz ultra-wideband receiver consisting of the LNA, I/Q mixers and the frequency synthesizer will also be sent for fabrication in May 2006.

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
GRADUATE FELLOWSHIP PROGRESS REPORT FALL 05

Project Name:	Cooperation in Large Wireless Networks
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Introduction:

In order for large networks to cooperate, we might need to transmit to destinations that are multiple hops away. Therefore, choice of a smart routing becomes necessary. Minimizing the total power in such systems is of paramount importance not just to increase its own operational lifetime in the case of battery powered devices, but also to coexist symbiotically with other systems which share the same frequency spectrum. For instance, 802.11 LANs and Blue-tooth networks share the same unlicensed band and can mutually benefit by limiting the power of their respective signal transmissions. Therefore, any proposed routing algorithm should be optimized in terms of power. Routing algorithms proposed for wireless networks are different from wired specifically because there is interference in wireless links. The existence of interference puts a lot of limits on data rate, and makes scheduling necessary in these networks. In our current work we are working on a joint routing and scheduling that optimizes power consumption.

Summary of Accomplishments:

We have studied optimization algorithms necessary for our work. Previously, people had to know all the transmission modes of the network in order to solve the optimal scheduling. The complexity of the corresponding algorithm is exponential, in general, in terms of the number of nodes in the network. We have partially developed an algorithm that iteratively calculates the optimal schedule without knowing the whole data. We have divided the big problem into master and slave sub-problems. Master problem solves the optimization with knowledge of a few of transmission modes, and the slave checks whether the answer given by the master is optimal.

On going work:

Most of the physical layer assumptions in the literature, in the field of joint routing scheduling is not precise. We would like to modify the communication assumptions. Also, we believe the assumption of knowing the whole traffic and solving the scheduling and routing is not practical. We want to solve the problem for the case of oblivious routing. In other words, we assume that we just know the space where the demand vector is located, and then come up with the routing and scheduling that consumes the least power; as opposed to knowing the exact value of the demand vector.

References:

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Project Name:	Signal Processing for Peak-to-Average Power Ratio (PAPR) Reduction and OBE Mitigation for MIMO-OFDM-Wireless Communication Systems
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Date:	March 29, 2006

Introduction: PAPR (Peak-to-Average-Power Ratio) Reduction is a serious problem in OFDM (Orthogonal Frequency Division Multiplexing) transmission over the wireless channel. For this reason, various PAPR reduction techniques have been proposed in the literature in the field. Obviously, all of these techniques have their own advantages and disadvantages. If we combine two different promising PAPR reduction techniques carefully, then it may be possible to get better performance with smaller distortion than by using any single one of them. This has motivated our following research.

Summary of accomplishments: In our Winter 06 research, we developed design criteria for combination of Clipping and Selective Mapping (SLM) in flat and frequency selective fading channels [1]. Clipping is one of the widely used and simplest PAPR reduction techniques for OFDM systems. However, both in-band distortion and out-of-band radiation can cause serious performance degradation. We assume that in-band distortion results in power loss and Gaussian noise, thus channel coding is very helpful for mitigation the effects of in-band distortion [2]. Out-of-band radiation can be removed by filtering. However, filtering should be used carefully since it causes peak re-growth [3]. Combining Clipping and SLM techniques was originally proposed in [2] for the Additive White Gaussian Noise (AWGN) channel using OFDM-QPSK. In [2], the authors used Nyquist-rate-sampled signal and showed Bit Error Rate (BER) performance in AWGN channel for several clipping ratios. Our work is different from [2] in several ways. First, over-sampling is important for PAPR reduction. We perform 4 times oversampling by using trigonometric interpolation. Without over-sampling, it is difficult to get an exact performance. Second, to mitigate, and also to measure spectral leakage, we use our recently developed Pre-Distorter in tandem with the HPA model. Third, we simulate and analyze PAPR reduction technique in flat and frequency selective fading channel conditions. Since OFDM is widely used for wireless channels, we believe fading channel analysis is more valuable than AWGN channel analysis. Finally, we propose design criteria depending on simulation results and analysis. The initial simulation result of combining clipping with SLM technique is given in Fig.1.

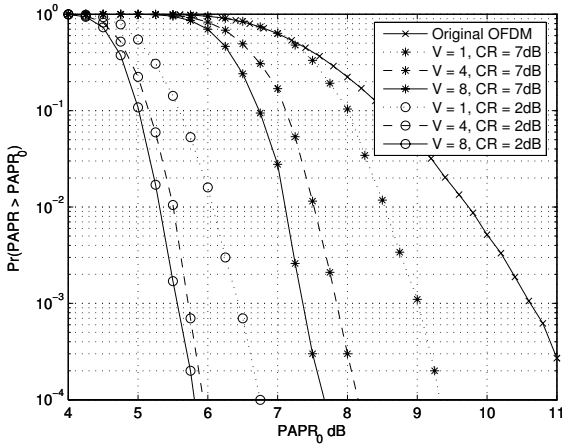

Fig.1. PAPR performance of clipping with SLM, CR (Clipping Ratio) = 2 and 7 dB

References:

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UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
CPCC Fellowship Winter Quarter Progress Report, April 2006

Project Name: **SOC Power Optimization Framework**
Graduate Student: **Sudeep Pasricha**, ICS (on CPCC Fellowship for Winter 2006)
CPCC Affiliate Professors: **Fadi J. Kurdahi** and **Nikil D. Dutt**

Project overview

The long term goal of the proposed project is to develop a system level methodology for power optimization for SoCs. In the immediate term, the proposed project will investigate techniques for efficient power modeling of SOC bus architectures, as well as of system-level IP blocks, and their use in the architectural exploration of IP-based SOC designs. On the basis of such power models of the system, we will be able to explore the architectural design space and evaluate various scheduling schemes. Meanwhile, the model is designed to be easily refined as the design process goes through the design flow, providing more accurate estimating of system performance and power consumption. The major purpose of the model is to provide a vehicle for researches on power optimization, such as the HAIM/DOSE (Hierarchically Abstracted IP modeling by Data Organization Space Exploration) exploration flow proposed earlier. The model and exploration flow are based on the COMMEX transaction-level communication architectural framework, on which we will study the H.264 application (the latest video coding standard), and JPEG2000 (the latest still image coding standard).

Progress

During Winter 2006, we engaged four students in this project and made steady progress. The student supported on CPCC Fellowship was Sudeep Pasricha, who focused on the SystemC modeling framework design as well as a case study of the H.264 decoder. Michael Shimasaki finished the RTL design of the H.264 Intra-Prediction module. Luis Bathen worked on JPEG2000 encoder modeling. Young-Hwan Park worked on the ASIC design task with the goal of providing us with important implementation data, and has successfully taken over and made changes to Yun Long's work, who graduated at the end of the fall quarter in 2005. During the winter quarter, we accomplished the following:

- Our research on system-level synthesis of bus matrix communication architectures for Multi-processor System-on-chips (MPSoCs) was presented at the *Asia and South Pacific Design Automation Conference* (ASPDAC) international conference held in Yokohama, Japan. This work, titled "Constraint-driven Bus Matrix Synthesis for MPSoC" received the **Best Paper Award** at the conference. The research paper proposed novel schemes to reduce the cost and development time of communication architectures for high performance electronic systems used in the next generation electronic devices such as mobile phones, video game consoles and high-speed networking equipment. This work was done using the SystemC modeling framework, and the system-level synthesis techniques being developed as part of the project.
- Our research on co-synthesis of memory and communication architectures at the system level, showed that co-synthesis allowed us to get better performance, compared to the traditionally used separate synthesis. Our research paper on this topic, titled "COSMECA: Application Specific Co-Synthesis of Memory and Communication Architectures for MPSoC" was accepted at the prestigious *Design Automation and Test in Europe* (DATE) 2006 conference, held in Munich, Germany. This paper was also invited for submission in a special issue of *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (IEEE TCAD) based on the best papers from DATE-2006.
- In our Sysplore tool, in order to have consensus between SystemC design and RTL design, we modified the SystemC code not to use global variables and partitioned tasks into software and hardware. Software tasks which will be performed by the CPU include control, setting, parameter calculation, address calculation and high level command, while hardware tasks which will be performed by the ASIC modules include execution intensive work such as 2D image processing, arithmetic and logical operation for massive data and block memory load and store. Four major ASIC blocks were identified: residual, intra prediction, inter prediction and deblocking filter block. All the partitioning of hardware and software blocks

for the four major blocks have been completed and test vectors for those blocks are also generated using the C code. This facilitates the design of the RTL blocks through a straightforward step of translating C code to Verilog or VHDL code and verifying the generated code with the test vectors. We also finished developing part of the module interface design (Master, Slave controller) and the internal block memories.

- We completed development of the SystemC model for JPEG 2000, based on the proposed architecture by Professor Kurdahi's group. We will soon start to port the existing JPEG2000 VHDL model to fit the same methodology used by the H.264 model, since the current implementation targets FPGAs. As porting of the VHDL model proceeds, required changes to the SystemC model will be made where necessary.
- We successfully finished creating a behavioral description of the H.264 intra-prediction module and are now working on integrating the design into the decoder. We will also synthesize the H.264 intra-prediction module into a gate-level design and create a set of test benches to compare the output of the behavioral model with the output of the gate-level model to ensure that both models are correct. We plan to have the RTL model of the decoder completed by the end of the Spring quarter and then subsequently begin the analysis of system power. This is a long-term task in parallel with our efforts on high-level modeling and optimization.

Going forward, our goal in 2006 is to finish the system model, integrating it with the performance and power data acquired from the ASIC design task, and study power optimization techniques with the help of easy design configuration of the model and accurate power modeling. The model should allow for easy and rapid migration to any multimedia application system. We will use the H.264 and JPEG2000 applications as drivers for this entire task.

Publications

1. Sudeep Pasricha, Nikil Dutt, Mohamed Ben-Romdhane, "Constraint-Driven Bus Matrix Synthesis for MPSoC", *Asia and South Pacific Design Automation Conference (ASPDAC 2006), Yokohama, Japan, January 2006* **(Best Paper Award)**
2. *S. Pasricha and N. Dutt, "A Framework for Memory and Communication Architecture Co-synthesis in MPSoCs," TR 06-03, February 2006.*
3. Sudeep Pasricha, Nikil Dutt, "COSMECA: Application Specific Co-Synthesis of Memory and Communication Architectures for MPSoC", *Design Automation and Test in Europe Conference (DATE 2006). Munich, Germany, March 2006*

Progress Report on MIMO Research: Winter 2006

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***Abstract*— We previously analyzed adaptive bit interleaved coded multiple beamforming (ABICMB) with the inclusion of adaptive modulation and coding over flat fading channels. Our aim was to exploit the channel state information further and achieve superior throughput performance compared to BICMB and the other spatial multiplexing techniques in the literature. In this study, we extend our previous work to frequency-selective channels with the help of orthogonal frequency division multiplexing (OFDM), and name the new system ABICMB-OFDM. Simulation results show that ABICMB-OFDM achieves significant performance gain compared to uniform BICMB-OFDM.**

I. Introduction

We previously showed that the diversity order of uncoded multiple beamforming decreases as more symbols are transmitted simultaneously [1]. The recent results in [2] show that if a properly designed bit interleaved coded modulation (BICM) is incorporated to the SVD-based multiple beamforming, one can achieve full spatial multiplexing of $\min(N, M)$ and full spatial diversity of NM for N transmit and M receive antennas over flat fading channels. However, bit interleaved coded multiple beamforming (BICMB) of [2] employs uniform power and constellation over the established subchannels. As a result, BICMB does not fully utilize CSI at the transmitter. In this work, we further exploit CSI with the inclusion of adaptive modulation and coding (AMC) in the system and maximize the throughput keeping the power level constant with a target bit error rate (BER). We especially focus on frequency-selective channels, and therefore use OFDM to combat ISI effects of multipath.

The analysis and the simulation results for both ABICMB and ABICMB-OFDM are combined and submitted as a journal paper to the IEEE Transactions on Wireless Communications.

II. Simulation Results

In the simulations below, the industry standard 64 states 1/2 rate (133,171) $d_{free} = 10$ convolutional code is used as the mother code. The rates $2/3$ and $3/4$ are constructed from the 1/2 rate mother code via puncturing. Therefore the cardinality of the encoder set used for adaptive loading is 3. The minimum Hamming distances are 10, 6 and 5 for the encoders respectively. For the high SNR region, we also allow uncoded adaptive loading to achieve rate 1, where the minimum Hamming distance is 1. The channel is assumed to be quasi-static and frequency-selective with Rayleigh distribution on each tap.

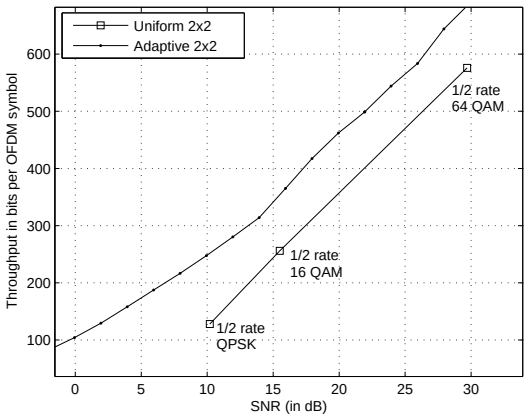

Fig. 1. Throughput performance of ABICMB-OFDM and uniform BICMB-OFDM for 2×2 antenna configuration at 10^{-5} BER in 50ns rms delay spread exponential channel.

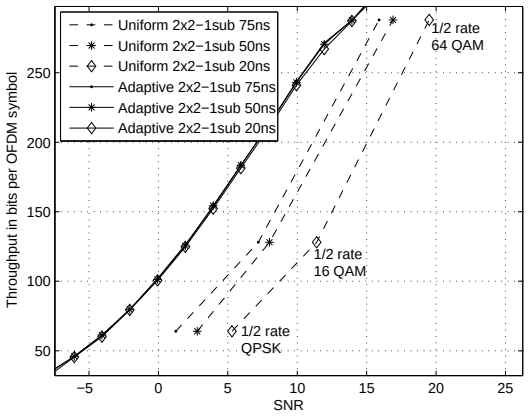

Fig. 2. Throughput performance of ABICMB-OFDM and uniform BICMB-OFDM for 2×2 antenna configuration at 10^{-5} BER for different rms delay spreads, where $\Gamma = 6.3$ dB.

Fig. 1 shows the performance results for ABICMB-OFDM and uniform BICMB-OFDM over a 50ns rms delay spread channel with 2×2 antenna configuration. As shown in Fig. 1, the adaptive system achieves 4-7 dB performance gain.

Fig. 2 demonstrates the robustness of the ABICMB-OFDM system against a change in the delay spread of the channel. In Fig. 2, only the largest singular value of the subcarriers are used for transmission, therefore adaptive loading is employed only over frequency. Actually, this is a performance

comparison of adaptive bit interleaved single beamforming and uniform bit interleaved single beamforming, which was previously analyzed in [3]. The adaptive system is robust against delay spread changes. As the delay spread decreases, the non-adaptive system has a performance loss, accordingly, the performance gain of the adaptive system increases.

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Project Name: Ultra-Low Power (ULP) Silicon-Based Analog/Mixed-Signal IC Design
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Address, Tel., e-mail; ET 644C, Irvine, CA, 92697-2625; (949)824-9324; payam@uci.edu
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Date: April 12, 2006

Introduction:

The ever increasing complexity of wireless communication transceivers makes the power minimization of accompanying RF front-end one of the most important design objectives. In particular, power minimization becomes crucial in emerging technologies such as body implanted sensors, radio frequency identification systems (RFID), and sensor networks, all of which requiring power consumption in microwatt range in order to enable the constituent transceiver to operate either without integrated power supply or at an extremely long battery-life.

Summary of Accomplishments:

We have made a good progress during the second quarter of this project. As we mentioned in the first quarter report, *the promise of this project is to radically change the way low-power circuits are designed*. Our submitted paper to the IEEE RFIC symposium 2006 was accepted. This paper investigated the use of CMOS technology to implement the ultra-low power (ULP) RF integrated circuits [1].

One of the main limitations in the ULP CMOS RFIC design is the low value of transistor's transconductance, g_m, due to the low bias current. Having already examined in low-power analog/digital ICs, an effective way of minimizing power consumption is to bias the transistor(s) in weak inversion region where the transistors achieve maximum value of g_m/I_D. Nonetheless, a weakly inverted transistor exhibits poor frequency response, and therefore, may not be used extensively in RFIC design. In our paper we studied the use of moderately inverted MOS transistors in ultra-low power (ULP) RFIC design. We introduced a new figure of merit for a MOS transistor, i.e., the $g_m f_T$-to-current ratio, ($g_m f_T/I_D$), which accounts for both the unity-gain frequency and current consumption during the optimization process of the transistor's performance. Using this figure of merit while taking into account the velocity saturation of short-channel MOS devices, it was shown both experimentally and analytically that the $g_m f_T/I_D$ reaches its maximum value in moderate inversion region. Moreover, we analytically investigated the noise behavior of the MOS transistor during the transition from weak inversion to strong inversion region. The measurement results were obtained for an NMOS transistor fabricated in Jazz Semiconductor's CMOS 0.18µm process.

In light of the analytical/experimental study presented in our IEEE RFIC symposium paper, we designed and fabricated three different RF amplifiers in CMOS 0.18µm and 0.13µm technologies. The RF transistors were biased in moderate inversion region to achieve maximum $g_m f_T/I_D$, which corresponds to achieving the maximum GBW for certain amount of bias current. We just completed measurement of one of the RF amplifiers. This circuit was designed to operate at 950MHz RF frequency.

The actual measurement results show a noise-figure (NF) of 4.9dB and a small signal gain of 15.6dB with a record-breaking power dissipation of only 100µW.

On going work:

As a continuation of our project, we are going to measure the other RF amplifiers, once the chips are back.

References:

[1] Amin Shameli, Payam Heydari, "Ultra-Low Power RFIC Design Using Moderately Inverted MOSFETs: An Analytical/Experimental Study" *to appear IEEE RFIC Symposium 2006.*

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
GRADUATE FELLOWSHIP PROGRESS REPORT SPRING 2005

Project Name:	Design Techniques Toward a Full-Rate 40Gb/s Transmitter in 0.18μm CMOS
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Student Fellowship Recipient:	Ahmad Yazdi

Introduction: Many bandwidth enhancement techniques have been developed to increase the speed of the CMOS ICs. We combined the distributed and lumped techniques to push the technology to the it's limit, enabling CMOS technology operating at 40Gb/s. We use push-push technique to generate 40GHz clock from second harmonic of 20GHz clock. The 20GHz clock is placed in a PLL loop.

Summary of Accomplishment:

The clock multiplying unit (CMU) is one of the major block in transmitter. A PLL with 1.25GHz reference clock has been designed. The VCO in the PLL loop is generating 20GHz clock. By two set of varactor in VCO, one is tuned by PLL and the other one is tuned by an off chip voltage, we achieved 18% tuning range on 20GHz. The effect of the varactor polarity in harmonic distortion of the *LC* VCO has been studied and verified by simulations.

On going Work:

1. Layout Post Layout Simulation: Post layout simulation includes RCX extraction for high speed blocks and 3D EM verification for the 40GHZ and 20GHz nodes in CMU.