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GRADUATE FELLOWSHIP PROJECTS PROGRESS REPORTS SPRING 2007

PROJECTS

ALPHABETIZED ACCORDING TO STUDENT LASTNAME

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KARIM EL DEFRAWY	Filter Allocation against DDoS Attachs	ATHINA MARKOPOULOU
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UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

GRADUATE FELLOWSHIP PROGRESS REPORT SPRING 07

Project Name: A Multi-Processor Architecture for Multimode Mobile Digital TV Platforms
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Introduction: As a base platform for NoC based system architecture, our NePA (*Ne*twork-based *P*rocessor *A*rray) [1] which are evolved from the previous MaRS (*Ma*cro-pipelined *R*econfigurable *S*ystem) will be used. Different from the original MaRS [2][2], the developed NoC architecture is applied and heterogeneous EU model which can be either programmable IPs or specific IPs is included. To support multiple standards in a single platform, the reconfigurability is an inevitable feature for the base platform.

Summary of Accomplishments: In the Spring Quarter 2007, a generic network interface (NI) for NePA platform and several tool chains were developed and associated paper was submitted [3][4]. Overall configuration of our tool chains is shown in Figure 1. Also as a prototype of homogeneous NePA system, the combined RTL codes were synthesized by Synopsys™ tools using Chartered™ 130nm processing technology. The physical characteristics of single PE are summarized in Table 1.

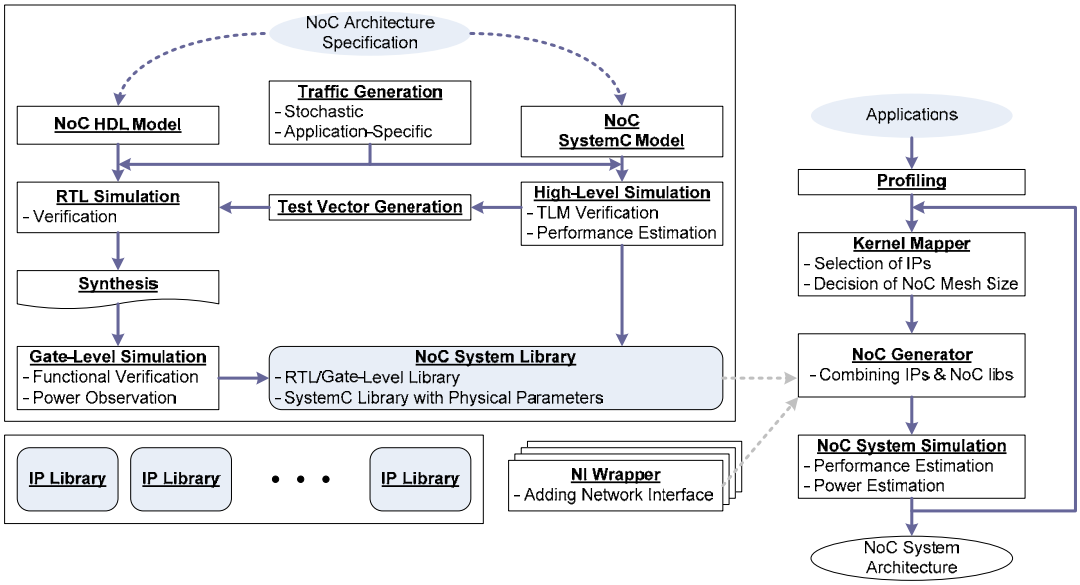

Figure 1. NePA tool chain

Table 1. Physical characteristics of single PE with CompactOpenRISC

		Router	FIFO		CompactOpenRISC			NI
			Depth 4	Depth 8	Data-RAM	Inst-RAM	Core	
Operating Voltage		1.0 V						
Operating Frequency		100 MHz						
Area (μm^2)		10,218	3,772	7,399	309,284	280,026	47,044	6,122
Power	Dynamic (mW)	2.52	4.25	8.20	206.8			2.78
	Leakage (μW)	1.86	1.17	2.30	27.31			2.24

On going work: In order to enhance the NePA platform, a generic NI will be refined for various type of IPs. And additional system benchmarks on homogeneous/heterogeneous NePA platform will be implemented.

Reference:

[1] Jun Ho Bahn et al., "On Design and Analysis of a Feasible Network-on-Chip (NoC) Architecture," *ITNG 2007*, pp.1033-1038, Apr. 2007
[2] N. Tabrizi et al., "MaRS: a Macro-pipelined Reconfigurable System," *Proc. Comp. Frontiers*, pp. 343 – 349, Apr. 2004.
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Improving DDoS Filtering Algorithms Progress Report - Spring 2007

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***Abstract*— During the spring of 2007, we continued our work on filter allocation against DDoS attacks [1]. We studied the structural properties of the optimal filter allocation and designed a heuristic that mimics the properties of the optimal solution. In addition, we used data logs (obtained through our other project [2]) to construct realistic distributions of bad traffic as input to our problem.**

I. Introduction

DDoS attacks are one of the most dangerous forms of attacks on the Internet. They are still largely unsolved, they threaten a lot of organizations and cause considerable financial losses. One defense mechanism currently used to defend against DDoS attacks is filtering attack flows at the routers using access lists. We have formulated the filter allocation problem as a resource allocation problem [1], and used a dynamic programming approach (DP) to find the optimal allocation. However, the complexity of the DP algorithm is prohibitive for real-time use. We developed an efficient algorithm, mimicking the structural properties of the DP solution, which is suitable for real-time operation.

The contributions during this quarter are the following:

- Studied the structural properties of the optimal filter allocation, i.e. how it depends on the distributions of the attack and legitimate traffic.
- Designed and evaluated a low-complexity heuristic, mimicking these structural properties.
- Analyzed the data logs from our BotTorrent work [2] to construct a realistic attack scenario (at the granularity of AS numbers and BGP prefixes). Used this scenario to test our algorithms for filter allocation.

II. Simulation Results

We simulated several different scenarios to evaluate our heuristic, and compare it to the optimal solution and the single-tier algorithms. Our simulation results show that the heuristic performs close to the optimal solution in a wide range of scenarios. The following subsections describe the details of each scenario and the simulation results.

A. Worm Distribution Simulations

In these scenarios, we simulated distributions of bad traffic behind gateways according to the infection distributions of worms (Code-Red [3], Slammer [4] and the Prolexic Zombie Report [5]). We observed that these are actually power-law distributions - some gateways contribute much more bad traffic than others. The developed heuristic performs well in all three cases. We also simulated the same scenarios for a large number of attackers and good users (more than a thousand attackers).

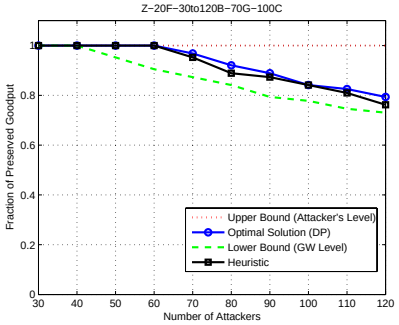

Fig. 1. Prolexic zombie report based attack simulation

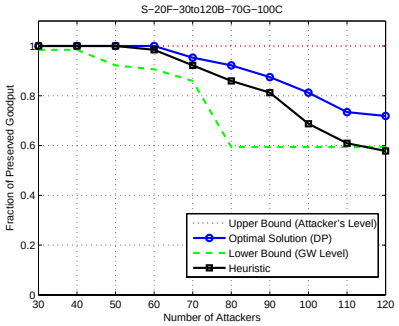

Fig. 2. Slammer based attack simulation

Fig. 1 shows the result of simulating the Zombie report-based attack with a small number of attackers and legitimate users. Figures 2 and 3 show the results for the same number of good and bad hosts behind each gateway but according to the slammer and code-red worms. Fig. 4 shows the results for the code-red distribution but with a large number of attackers.

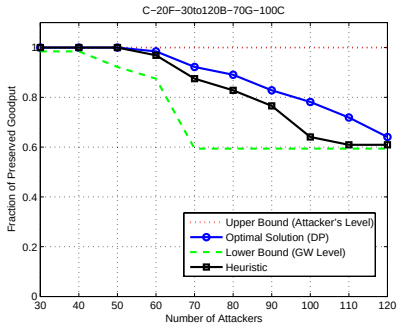

Fig. 3. Code-Red attack based simulation

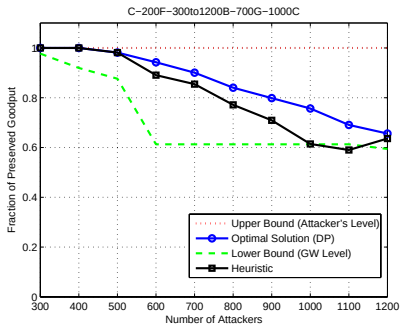

Fig. 4. Code-Red attack based simulation with large number of attackers

B. BotTorrent Distribution Simulations

This scenario captures a distribution of bad nodes behind gateways similar to the attacking IPs we measured in our BotTorrent experiments [2]. We mapped IPs from our experiments to their corresponding BGP prefixes (and autonomous systems (ASs). In our data logs, there were roughly 2400 ASs and the number of IPs seen from each AS followed a power-law distribution. Over 2000 of these ASs contained only one attacking IP in them. Similar analysis was done on mapping the IPs to announced BGP prefixes. Over 12000 BGP prefixes were mapped and over 10000 of these BGP prefixes had only one IP in them. Both results show a power-law behavior in the number of ASs and BGP prefixes. We are currently analyzing the results from these simulations.

III. Future Work

So far, we studied the problem of filter allocation for two-tiers of aggregation against a static (instance of) attack. Next steps include:

- Design an algorithm that adapts to dynamic attacks. It is desirable that the optimal allocation can be incrementally updated to amortize prior work.
- Study the problem of filter allocation to several customers (i.e. several victims of DDoS attacks).
- Move from a two-tiers topology to the general problem of placing filters anywhere in the attack tree.

Note: Beyond the progress on the problem itself, this project led to two additional developments in our group:

- It led to a collaboration with AT&T Research. Karim El Defrawy is currently on an internship with the Networking Group in NJ, studying how to improve the efficiency of filtering services provided to AT&T customers. We expect that this project will continue in Prof. Markopoulou's group for the next year in collaboration with AT&T.
- In the winter quarter, Karim El Defrawy together with Minas Gjoka, another student in the group, demonstrated the potential misuse of BitTorrent for launching DDoS attacks, as described in our winter progress report [2]. Apart from feeding realistic data into the filtering work, BotTorrent is a project in itself, and attracted the interest of media such as NewScientist and Slashdot.

We are grateful to CPCC for the support during 2006-2007 that enabled our group to initiate multiple threads in the research area of DDoS and unwanted traffic.

References

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[3] D. Moore, C. Shannon, J. Brown, "Code-Red: a case study on the spread and victims of an Internet worm", *in Proc. ACM IMW 2002.*

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CPCC Progress Report, Spring 2007

Joint Source-Channel Coding and Quantized Feedback for Quasi-Static Fading Channels

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Our research is motivated by the recent demand for multimedia content delivery over wireless channels. Unlike data transmission systems where the objective is to minimize the bit errors, the design objective in multimedia transmission systems is to reduce the expected distortion of the received signal. In this context, the Shannon's separation theorem states that under an infinite block length assumption, the source and channel coding tasks can be performed separately. The latter assumption is easily violated in delay-sensitive and power-limited applications such as the case for slowly fading channels. Thus, we study joint source-channel coding approaches to this problem.

We consider a scenario where the delay constraint limits coding to a single block of fading. The reliable transmission rate, or the mutual information, then becomes a random variable and outage occurs if the transmission rate is larger than the mutual information. Our previous work considered a scenario where only the receiver has knowledge about the channel and time-sharing or superposition coding strategies were used to deal with the channel uncertainty [1], [2]. We also considered the case where a low-rate, noiseless feedback channel is available from the receiver to the transmitter. We studied the joint source-channel coding problem from both the finite-SNR and high-SNR perspectives [3].

Our more recent work has focused on the case where the feedback channel suffers from noise. Noisy feedback introduces an additional source of error into the system that is caused by the possibly incorrect channel state information at the transmitter. Therefore, the design objective here is to ensure that the system performance with noisy feedback is always somewhere between that of the no-feedback and noiseless feedback systems. The effects of noisy feedback on the system performance were incorporated into the system design by using a channel optimized scaler quantizer (COSQ). We proposed an efficient numerical technique for COSQ design and power adaptation at the transmitter. Figure 1 shows the expected distortion of the proposed system for different values of the feedback channel bit error rate ε. It can be seen from the Figure that the COSQ performance is close to the no-feedback system for large values of ε and approaches that of noiseless feedback for small ε.

We also investigated the asymptotic performance of the noisy feedback system based on the distortion exponent that is defined as $\Delta = -\lim_{SNR\to\infty} \frac{\log \mathcal{E}_D}{\log SNR}$. We proved the following result in this context.

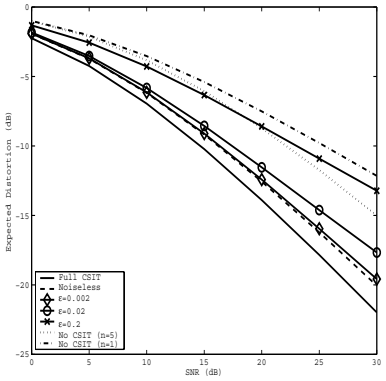

Fig. 1. Expected distortion for a 1×1 system with $K = 8$, $b = 1$ and a short-term power constraint

Theorem: The distortion exponent of the system with noisy feedback is

$$\Delta = \frac{bM}{b+M} \tag{1}$$

that is the same as the distortion exponent of a single-layer no-CSIT system ($K = 1$). In this equation, b is the bandwidth expansion ratio and M is the number of receive antennas in a single-input, multiple-output (SIMO) scenario.

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[3] F. Etemadi, H. Jafarkhani, "Joint Source-Channel Coding for Quasi-Static Fading Channels with Quantized Feedback," *IEEE International Symposium on Information Theory*, June 2007.

[4] F. Etemadi, S. Ekbatani, H. Jafarkhani, "Joint Source-Channel Coding for Quasi-Static Fading Channels with Noisy Quantized Feedback, *IEEE Information Theory Workshop*, September 2007.

CPCC Fellowship Progress Report, Spring 2007:

Combining Beamforming and Space-Time Block Coding over Reconfigurable MIMO

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I. Overview

In this report, we consider a Reconfigurable MIMO (REMIMO) system where some Channel State Information (CSI) is available at the transmitter. Depending on the quality of the channel information at the transmitter, various transmission schemes are possible. For example, one possible closed loop scheme is when we have $\log P$ bits feedback, where P is the number of states at the transmitter, and based on these feedback bits we choose the best state of the transmit antenna and fix the state throughout the transmission scheme. Authors in [1], consider the channel estimates as side information at the transmitter and adapt the existing space time block codes to the CSI. In this report we follow a similar approach as [1].

II. Problem Formulation

Assume we have N transmit and M receive antennas, where the transmit antennas are reconfigurable with P radiation states. We follow the system model described as $\mathbf{Y} = \mathbf{CH} + \mathbf{N}$, where, $\mathbf{C} = \text{diag}\{\mathbf{C}_1, \mathbf{C}_2, \ldots, \mathbf{C}_P\} \in \mathcal{C}^{PT \times PN}$ is the transmitted codeword, $\mathbf{Y} \in \mathcal{C}^{PT \times M}$ is the received matrix, $\mathbf{H} \in \mathcal{C}^{PN \times M}$ is the channel matrix and $\mathbf{N} \in \mathcal{C}^{PT \times M}$ is a zero-mean Gaussian noise matrix. In [1], a new performance criterion for space-time block codes is given which takes the knowledge of channel estimates into account.

$$\ell(\mathbf{C}^k, \mathbf{C}^l) = \mathbf{m}^*_{\mathbf{h}|\hat{\mathbf{h}}} \mathbf{R}^{-1}_{\mathbf{hh}|\hat{\mathbf{h}}} \mathbf{\Psi}(\mathbf{C^k}, \mathbf{C^l})^{-1} \mathbf{R}^{-1}_{\mathbf{hh}|\hat{\mathbf{h}}} \mathbf{m}_{\mathbf{h}|\hat{\mathbf{h}}} - \log\det(\mathbf{\Psi}(\mathbf{C^k}, \mathbf{C^l})) \quad (1)$$

where, $\mathbf{h} = \mathbf{vec}(\mathbf{H})$ and $\mathbf{\Psi}(\mathbf{C}^k, \mathbf{C}^l) = I_{PQN} \otimes A(\mathbf{C}^k, \mathbf{C}^l)/4\sigma^2 + \mathbf{R_{hh}}^{-1}$, where $\mathbf{R_{hh|\hat{h}}}$ is the actual channel covariance matrix given the channel estimates. We set the transmission scheme to be a linear transformation of each STBC codeword sent out during each channel propagation state: $\mathbf{C}_p = W_p \overline{\mathbf{C}}_p, \quad p \in \{1, \ldots, P\}$, where, $\overline{\mathbf{C}}_p$ is the predetermined STBC code word. Assume $\mathbf{R_{hh|\hat{h}}} = \alpha I_{NMP}$. We can rewrite $\ell(\mathbf{C}^k, \mathbf{C}^l)$ as,

$$\sum_{p=1}^{P} tr\{(\frac{\mu_p^{kl}}{4\sigma^2} W_p W_p^H + \frac{1}{\alpha} I_N)^{-1} (\frac{\gamma_{i1} + \gamma_{i2} + \cdots + \gamma_{iM}}{\alpha^2})\} - M \sum_{p=1}^{P} \log\det\left(\frac{\mu_p^{kl}}{4\sigma^2} W_p W_p^H + \frac{1}{\alpha} I_N\right) \quad (2)$$

where, $A(C_p^k, C_p^l) = \mu_p^{kl} I_N$ for $p \in \{1, \ldots, P\}$. Now, let $Z_p = W_p W_p^H$ and let γ_{pm} denote the $N \times N$ blocks on the diagonal of $m_{h|\hat{h}} m_{h|\hat{h}}^H$.We can rewrite Eq. (2) as follows

$$\ell(Z_1, \ldots, Z_P) = -M \sum_{p=1}^{P} \log\det\left(\frac{\mu_p^{kl}}{4\sigma^2} Z_p + \frac{1}{\alpha} I_N\right) + \sum_{p=1}^{P} tr\{(\frac{\mu_p^{kl}}{4\sigma^2} \alpha Z_p + I_N)^{-1} (\frac{\gamma_{i1} + \gamma_{i2} + \cdots + \gamma_{iM}}{\alpha})\} \quad (3)$$

Now the optimization problem is

$$\min_{\substack{Z_p: \text{ positive def.} \\ tr(Z_p)=1}} \ell(Z_1, \ldots, Z_P) \quad (4)$$

Equation (4) is a convex optimization problem with respect to Zp's, therefore the existing methods such as interior point methods can be used to solve the problem. In this section, we attempt to find a closed form solution to the above optimization problem. Generally, the approach is to minimize the maximum value of $\ell(Z_1, \ldots, Z_P)$ taken over all codeword pairs, but here it is not straight forward to decide the maximum of $\ell(Z_1, \ldots, Z_P)$ in terms of μ_p^{kl}'s, unless we make some additional assumptions. Therefore, the fact that μ_p^{kl}'s can not be independently minimized, turns the problem into a complex min-max optimization problem. Let us make the simplifying assumption that the maximum of $\ell(Z_1, \ldots, Z_P)$ is achieved when $\mu_1^{kl} = \mu_2^{kl} = \ldots = \mu_P^{kl} = \mu_{min}$, therefore

$$\ell(Z_1, \ldots, Z_P) = \sum_{p=1}^{P} \left(tr\{(\frac{\mu^{min}}{4\sigma^2} \alpha Z_p + I_N)^{-1} \Upsilon\} - M \log\det\left(\frac{\mu^{min}}{4\sigma^2} Z_p + \frac{1}{\alpha} I_N\right)\right) \quad (5)$$

where, $\Upsilon = \frac{\gamma_{i1} + \gamma_{i2} + \cdots + \gamma_{iM}}{\alpha}$. Now, each term in the optimization problem can be independently minimized. The solution to the above optimization problem is given by algorithm in [1].

1) Set $l = 1$
2) Solve for the Lagrange multiplier μ from $1 + \frac{N-l+1}{\alpha \frac{\mu_{min}}{4\sigma^2}} - \sum_{k=l}^{N} \frac{\alpha \frac{\mu_{min}}{4\sigma^2} M + \sqrt{\alpha^2 \frac{\mu_{min}^2}{16\sigma^4} M^2 + 4\alpha \frac{\mu_{min}}{4\sigma^2} \hat{\lambda}_k \mu}}{2\alpha \frac{\mu_{min}}{4\sigma^2 \mu}} = 0$
3) calculate λ_i's (the eigenvalues of Z_p) from $\lambda_i = \frac{\alpha \frac{\mu_{min}}{4\sigma^2} M + \sqrt{\alpha^2 \frac{\mu_{min}^2}{16\sigma^4} M^2 + 4\alpha \frac{\mu_{min}}{4\sigma^2} \hat{\lambda}_i \mu}}{2\alpha \frac{\mu_{min}}{4\sigma^2 \mu}} - \frac{1}{\alpha \frac{\mu_{min}}{4\sigma^2}}$
4) If $\lambda_i < 0$ set $\lambda_i = 0$, $l = l + 1$ repeat from 2
5) Compute $W_p = \hat{V} \Lambda^{1/2}$, where $\Upsilon = \hat{V} \hat{\Lambda} \hat{V}^H$

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Optimal Two-way Relaying with Half-duplex Relays

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I. Introduction

Cooperation and relaying in wireless networks offer enormous throughput enhancement by creating a virtual MIMO. However, one of the major limitations with relaying is the half duplex constraint at the relays, wherein the relays cannot transmit and receive simultaneously. This leads to a significant loss in spectral efficiency. Typically, for two hop relaying, the spectral efficiency loss is 50% compared to full duplex relaying [1]. Due to the broadcast nature of the wireless medium, Shannon's two way channel [2] where two users communicate to each other through a common channel, is well suited to wireless relay networks. Therefore, by employing two way relaying, the spectral efficiency loss due to half duplex constraint can be recovered to some extent.

II. System Model and Problem Statement

We consider a dual-source parallel relay network as shown in Fig. 1. In this model, two user nodes U_1 and U_2 wish to communicate to each other through a set of N half-duplex relays. Note that there is no direct link between the users. Here each source has power P_k, $k = 1, 2$ and the relays have

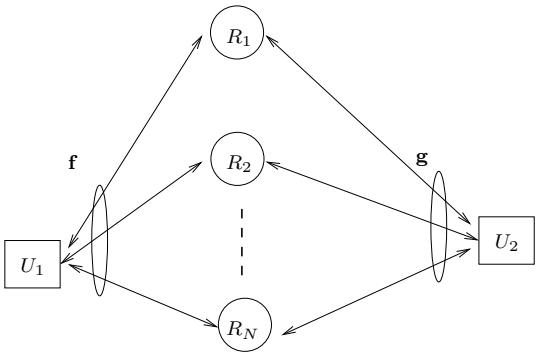

Fig. 1. Two-hop Two-way Parallel Relay Network

a sum power constraint of P_R. The $N \times 1$ vectors $\mathbf{f}$ and $\mathbf{g}$ represent the channels between the users and the relays. Due to the half-duplex nature of the relays, communication takes place in two slots. We assume quasi-static fading with global channel knowledge at all nodes. Further, we assume that the sources employ Gaussian signalling at their peak power. In the first time slot, the sources transmit x_1 and x_2 respectively. The relay received symbols during the first time slot are given by

$$\mathbf{r} = \mathbf{f}x_1 + \mathbf{g}x_2 + \mathbf{n_R} \tag{1}$$

where the elements of $\mathbf{n_R}$ are i.i.d. AWGN with unit variance. In the second slot, the relays amplify their received signal subject to the sum power constraint of the relays which is given by

$$\sum_{i=1}^{N} |d_i|^2(|f_i|^2P_1 + |g_i|^2P_2 + 1) = P_R \tag{2}$$

where $\mathbf{d} = [d_1\ d_2 \cdots d_N]$ is the relay amplification vector. During the second slot, U_1 receives

$$y_1 = \left(\sum_{i=1}^{N} f_i^2 d_i\right) x_1 + \left(\sum_{i=1}^{N} f_i g_i d_i\right) x_2 + \sum_{i=1}^{N} f_i d_i n_{R_i} + n_{U_1} \tag{3}$$

As U_1 knows its transmitted symbol x_1, it can cancel out the terms associated with x_1 before decoding x_2. The received signal at U_2 is

$$y_2 = \left(\sum_{i=1}^{N} g_i f_i d_i\right) x_1 + \left(\sum_{i=1}^{N} g_i^2 d_i\right) x_2 + \sum_{i=1}^{N} g_i d_i n_{R_i} + n_{U_2}. \tag{4}$$

As before, x_2 can be canceled before decoding x_1. Therefore, for any relay amplification vector $\mathbf{d}$, the achievable rates are given by

$$R_1 = \log\left(1 + \frac{|\sum_{i=1}^{N} f_i g_i d_i|^2 P_1}{1 + \sum_{i=1}^{N} |d_i g_i|^2}\right) \tag{5}$$

$$R_2 = \log\left(1 + \frac{|\sum_{i=1}^{N} f_i g_i d_i|^2 P_2}{1 + \sum_{i=1}^{N} |d_i f_i|^2}\right). \tag{6}$$

We seek to determine the set of all possible achievable rates $(R_1,\ R_2)$ that can be supported simultaneously under a sum power constraint at the relays.

Theorem 1: The relay amplification vector that maximizes any linear combination of rates $\mu_1 R_1 + \mu_2 R_2$ has the following structure.

$$d_i = \frac{\gamma f_i^* g_i^*}{D_1(i)\sin\theta + D_2(i)\cos\theta}, \qquad i = 1, 2...N \tag{7}$$

where

$$D_1(i) = \left(|f_i|^2P_1 + |g_i|^2(P_R + P_2) + 1\right)$$
$$D_2(i) = \left(|f_i|^2(P_1 + P_R) + |g_i|^2P_2 + 1\right)$$

and γ is necessary to satisfy the relay power constraint. ■

This result allows us to characterize all possible rate pairs that can be simultaneously supported. The resulting rate region is shown in Fig. 2. Here $\theta = 0$ maximizes the rate of User 1, while $\theta = \pi/2$ maximizes R_2. For all other linear combination of rates, θ takes a value from $[0, \pi/2]$. For the important case of sum rate $R_1 + R_2$, θ can be numerically optimized to

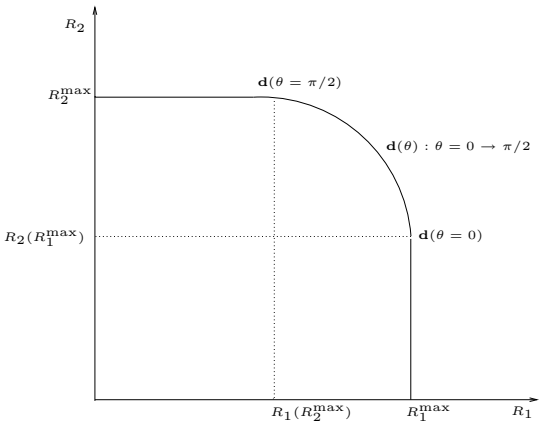

Fig. 2. Rate Region: Two-way parallel AF relay network

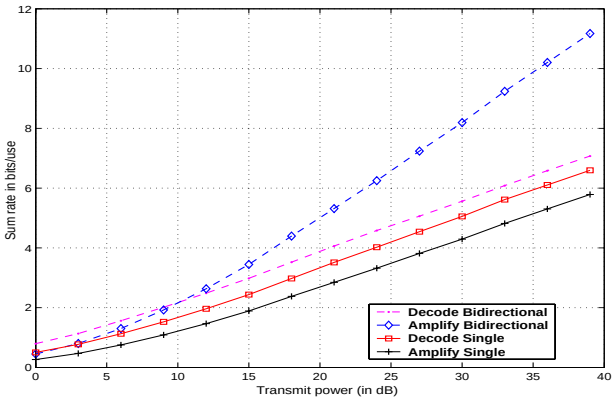

Fig. 3. Average rate of the two way channel in Fig. 1 as a function of transmit power $P_1 = P_2 = P_R$ for $N = 2$.

determine the optimal relay amplification factors. Notice that the N-dimensional relay optimization problem is reduced to a one dimensional optimization problem.

Fig. 3 shows the sum-rate of AF and DF for both one-way and two-way relaying as a function of transmit power of the nodes. For DF, we utilize the link scheduling model used in [3]. For the one way channel, DF is superior to AF. This is surprising as AF is more suited to parallel relay networks than DF. However, the link scheduling based DF outperforms AF due to the half duplex constraint of the relays. With AF, the destination requires two time slots to receive one symbol, i.e. only one hop is active at any time slot. However for the two-way channel, AF significantly outperforms DF. This is because two way relaying helps AF exploit both the hops efficiently. Here, each user receives one symbol in two time slots and thereby spectral efficiency is increased two-fold.

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CPCC 2006 Spring Quarter Report: Design of MEMS-reconfigurable decoupling networks for closely-spaced multi-element antennas in MIMO systems.

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I. Introduction

In today's wireless communication applications, compact and efficient antennas/arrays are required to satisfy the spacing requirements arising from multi-element antenna architectures (beamforming switching, multiple input multiple output, etc) and for integration purposes with other radio modules. Closely-spaced antennas suffer from mutual coupling which is a detrimental electromagnetic phenomenon that reduces the efficiency of the antennas. External decoupling networks can be used to compensate the mutual coupling among the antennas such that a good efficiency can be achieved over a reasonable frequency band.

As seen by the author, for a given antenna array geometry, the design of the decoupling networks is not unique. This opens the possibility to build MEMS-reconfigurable decoupling networks that while decoupling closely-spaced antennas, they are also simultaneously able to produce a set of uncorrelated radiation patterns/modes. This reconfigurable capability can be used in a MIMO [1] system to further enhance its performance.

II. Past Achievements (Fall Quarter)

During the fall quarter we developed a methodology for the design of specific decoupling networks for different antenna array topologies that are suitable to be made reconfigurable through MEMS technology. This methodology is based on the Generalized Takagi Decomposition of the measured Scattering Parameters matrices of the arrays. For the seek of knowledge, a Scattering Matrix is a matrix that relates the voltage wave incident on the ports to those reflected from the ports, and is normally measured directly with a vector network analyzer [2][3]. As shown by the authors, the Takagi factorization, provides a methodology to design decoupling networks that are reciprocal, that is, physically realizable, for any MEA structure. The multiplicity of the eigenvalues of the factorization is an indicator of the number of different decoupling networks that exist for a given array configuration.

III. Past Achievements (Winter Quarter)

During the winter quarter we concentrated our efforts on the physical implementation, with microstrip technology, of reconfigurable decoupling networks for circular arrays of closely-spaced antennas. In particular, we have started the design of a reconfigurable decoupling network for a circular array of two antennas and two distinct networks for a circular array of four antennas. The antennas are separated a distance of 0.14λ.

In particular for the circular array of two antennas, the resultant network uses one 180° hybrid followed by a switching network composed of several MEMS-switches. On the other hand, for the circular array of four antennas, one of the realized network designs uses four 180° hybrids, while a second network design uses three 180° hybrids. Both networks are followed by a switching network which is made out of several MEMS-switches.

The decoupling network plus the switching circuitry form a MEMS-reconfigurable decoupling network which have the capability to change the radiation state of the antenna array.

IV. Current Achievements (Spring Quarter)

During this quarter we have finalized the design and optimization of the decoupling networks for the 2x1 linear array (or 2 element circular array) and for the 2x2 planar array (or four element circular array). We have also finalized the design phase of the switching circuitry, which employs MEMS switches to commute two input lines into one single output line. Both the networks and switching circuitry are now in the fabrication stage. A picture of the mask used for the fabrication of the aforementioned circuits is shown in Fig. 1.

Through simulations we have computed the radiation pattern and scattering parameters of the antenna array when connected to the proposed decoupling networks, as shown in Fig. 2. We are currently conducting measurements on the radiation pattern and scattering parameters. Those measurements are obtained using the laboratory equipment, such as: HP 8510 2-50GHz network analyzer, and a conical compact anechoic chamber.

We are also currently in the process of writing an journal paper to be submitted to the IEEE Transactions on Antennas and Propagation.

V. Future work

By means of combining the decoupling capabilities of the proposed networks with the reconfigurable capabilities introduced by the MEMS-switches, the resultant networks can

be made to produce a set of orthogonal radiation patterns among its ports and among its different states. This is a novel capability that can be used to improve the performance of current MIMO systems. That is, the circular array of two antennas can therefore be seen as a single-port multi-antenna system that can radiate in two different states, where in each state the input port can be associated with a different orthogonal radiation pattern. Similarly, the four antennas circular array can be seen as a two-ports multi-antenna system that can radiate in two different states. Once again, the two different sets of radiation patterns, associated with the two input ports, are orthogonal among each other.

Finally we will conduct system level simulations using MATLAB to find out the capacity and BER of the new proposed system, as well as specific experiments to obtain the system capacity and diversity order of the proposed multi-antenna system, once fabricated.

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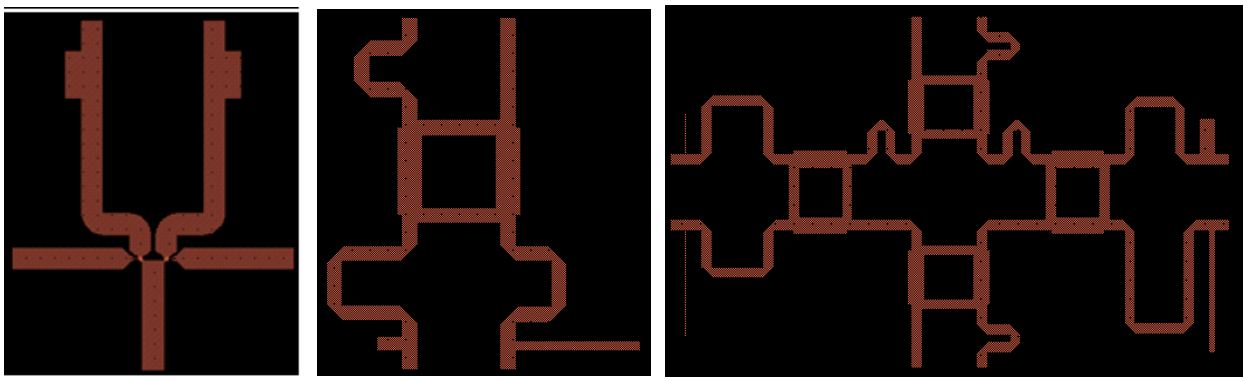
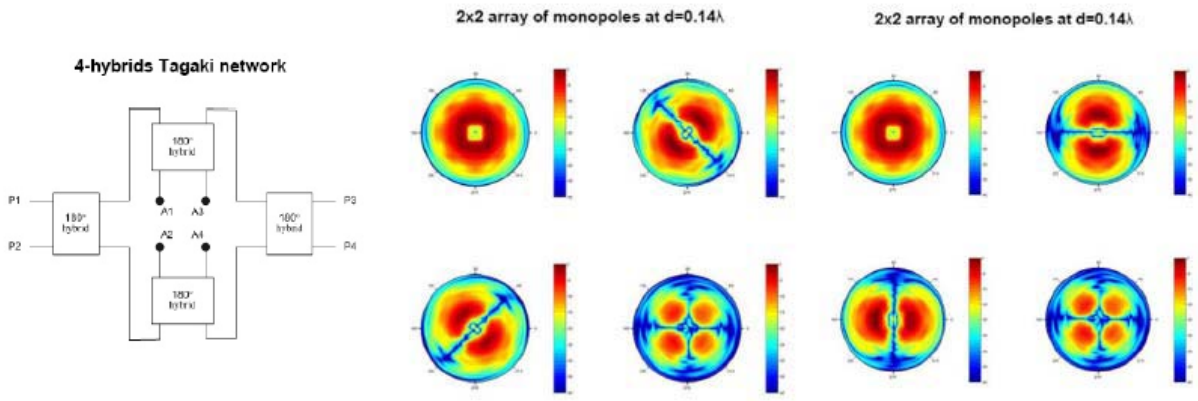


(a) SWITCHING CIRCUITRY

(b) TAKAGI NETWORK (2x1 array)

(b) TAKAGI NETWORK (2x2 array)

Fig. 1. Microstrip implementation of the decoupling network of the two antennas circular array generated using the Tagaki factorization.



(a) Schematic TAKAGI NETWORK (2x2 array)

(b) Radiation patterns TAKAGI NETWORK (2x2 array)

Fig. 2. Microstrip implementation of the switching network with four MEM switches on it.

Multimedia Capacity Analysis of the IEEE 802.11e Contention-based Infrastructure Basic Service Set

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I. Introduction

This quarter, we completed the design of a simple mathematical analysis framework for the Enhanced Distributed Channel Access (EDCA) function of the recently ratified IEEE 802.11e standard [1]. Our analysis considers the fact that the distributed random access systems exhibit cyclic behavior. The proposed model is valid for arbitrary assignments of AC-specific Arbitration Interframe Space (AIFS) values and Contention Window (CW) sizes and is the first that considers an arbitrary distribution of active Access Categories (ACs) at the stations. Validating the theoretical results via extensive simulations, we show that the proposed analysis accurately captures the EDCA saturation performance.

Next, we designed a framework for multimedia capacity analysis of the EDCA function. We calculate an accurate station- and AC-specific queue utilization ratio by appropriately weighing the service time predictions of the cycle time model for different number of active stations. Based on the calculated queue utilization ratio, we design a simple model-based admission control scheme. We show that the proposed call admission control algorithm maintains satisfactory user-perceived quality for coexisting voice and video connections in an infrastructure BSS and do not present over- or under-admission problems of previously proposed models in the literature.

II. EDCA Cycle Time Analysis

We propose an average cycle time analysis to model the behavior of the EDCA function of any AC at any station. This model is an enhanced version of our previous design [2]. The key improvement is that the proposed cycle time model is valid for an arbitrary distribution of active Access Categories (ACs) at the stations. We first define a Traffic Class (TC). Then, we derive the TC-specific average collision probability. Next, we calculate the TC-specific average cycle time. Finally, we relate the average cycle time and the average collision probability to the normalized throughput and service time.The interested reader is referred to [3] for the mathematical formulation of the model.

We validate the accuracy of the numerical results obtained from the analytical model by comparing them to the simulation results obtained from ns-2 [4]. For the simulations, we employ the IEEE 802.11e HCF MAC simulation model for ns-2.28 [5]. In simulations, we consider two ACs, one high priority (AC_3) and one low priority (AC_1). Unless otherwise stated, each station runs only one AC. We set $AIFSN_1 = 3$, $AIFSN_3 = 2$, $CW_{1,min} = 31$, and $CW_{3,min} = 15$. For both ACs, the payload size is 1000 bytes. RTS/CTS handshake is turned on. All the stations have 802.11g Physical Layer (PHY) using 54 Mbps and 6 Mbps as the data and basic rate respectively.

We test the performance of the system when the stations run multiple ACs so that virtual collisions may occur. The stations run only AC_1, only AC_3, or both. We define TC_0 as the AC_3 when only AC_3 is active at the station, TC_1 the AC_3 when both AC_3 and AC_1 are active at the station, TC_2 as the AC_1 when only AC_1 is active at the station, and TC_3 the AC_1 when both AC_3 and AC_1 are active at the station. We keep both N_1 and N_3 at 10 (N denotes the total number of stations using the corresponding AC), and vary the number of TC_1 and TC_3 from 0 to 10 (therefore, TC_0 and TC_2 vary from 10 to 0). Fig. 1 shows the normalized throughput of each TC. The predictions of the proposed analytical model follow the simulation results closely. Although not significant for the tested scenario and not apparent in the graphical results, a closer look on the numerical results present the (slightly) higher level of differentiation between AC_3 and AC_1 which is due to the additional prioritization introduced at the virtual collision procedure.

III. Voice Capacity Analysis

When working in the saturated case, the contention-based 802.11 MAC suffers from a large collision probability, which leads to low channel utilization and excessively long delay. As shown in [6], the optimal operating point for the 802.11 to work lies in nonsaturation where contention-based 802.11 MAC can achieve maximum throughput and small delay. In [7], it is also shown that a very small increase in system load yields a huge increase (of about two orders of magnitude) of the backoff delay. When the traffic load does not exceed the service rate at saturation, the resulting medium access delay is very small.

We propose a novel framework where we calculate TC-specific average frame service rate μ via a weighted summation of saturation service rate $E[t_{srv}]$ over varying number of active stations. Defining a TC-specific average queue utiliza-

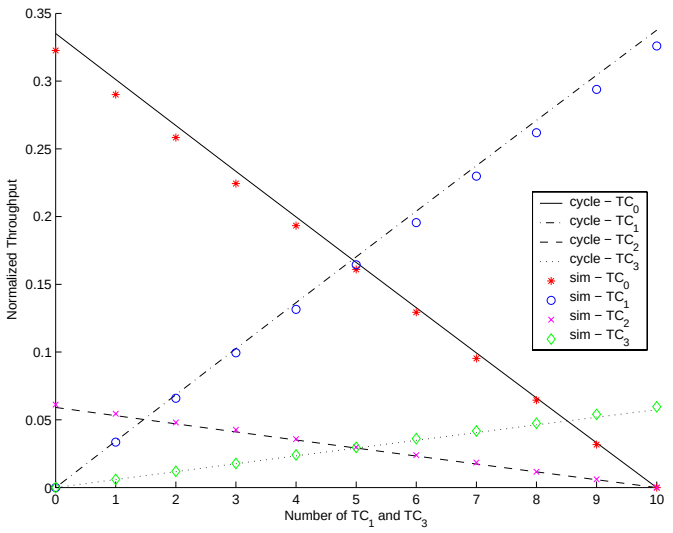

Fig. 1. Analytically calculated and simulated performance of each TC when the number of TC_1 and TC_3 is varied from 0 to 10 (therefore, TC_0 and TC_2 vary from 10 to 0).

tion ratio ρ, we design a simple call admission control algorithm which limits the number of admitted realtime multimedia flows in the 802.11e infrastructure BSS in order to prevent the corresponding TC queues going into saturation. Admitted realtime multimedia flows can be served with QoS guarantees, since low transmission delay and packet loss rate can be maintained when the 802.11e WLAN is in nonsaturation [6],[7]. Comparing with simulation results, we show that not only does the proposed admission control algorithm prevent the so-called over-admission or under-admission problems but also efficiently utilizes the network capacity. The interested reader is referred to [3] for the details on the design of the framework.

For performance validation via simulations, we consider an infrastructure BSS. All the stations including the AP use the suggested EDCA parameters in [1]. The voice traffic model implements G.711 or G.729 VoIP application as Constant Bit Rate (CBR) traffic. The voice codec parameters are selected as in [8]. We use a network topology such that a voice connection is initiated between a distinct party in the Internet and the WLAN. The traffic is relayed at the AP from (to) the wireless channel to (from) the wired link. The wired link delay is set to 20 ms for all connections.

We investigate the VoIP capacity of 802.11e WLAN when no other type of traffic coexists. A two-way voice connection is established every ω ms, with the starting time randomly chosen over $[0, \omega]$ ms. We set ω equal to the packet interval duration of the voice codec used. Table I tabulates the maximum number of VoIP connections for different codecs. In the simulations, the maximum number of voice connections is obtained in such a way that one more connection results in the delay outage ratio (the ratio of the number of audio packets with end-to-end delay exceeding 150 ms over the total number of packets transmitted) larger than 1% [8]. As shown in Table I, the analytical results for the proposed model and the simulation results closely follow each other. The obtained analytical

TABLE I
COMPARISON OF THE MAXIMUM NUMBER OF VOIP CONNECTIONS

Audio	G.711		G.729	
(ms)	Analysis/Simulation	[8]	Analysis/Simulation	[8]
10	27/27	21	29/29	22
20	49/49	38	56/56	43
30	70/70	53	85/85	65
40	87/87	67	112/112	85
50	102/102	79	139/139	106
60	115/115	89	166/166	128

bounds are much tighter when compared to the results obtained using the model in [8]*. As the comparison of the performance with 802.11e MAC parameters in 802.11g PHY layer indicates the model in [8] has significant under-admission problems for an arbitrary selection of MAC parameters (especially when the CW settings are small and the underlying PHY is 802.11g).

The interested reader is referred to [3] for more details and simulation results.

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*Our implementation of the model in [8] duplicates the analytical results in [8] which are for a specific DCF MAC parameter set. Although the results are not provided in this paper, the analytical results for the proposed model and our simulation results also confirm the capacity prediction of [8] for the specific DCF scenario.

UC Irvine Center For Pervasive Communications and Computing Graduate Fellowship Progress Report Spring 2007

July 3, 2007

Project Name: Adaptive Equalization of Multimode Fiber Channels in 0.18μm CMOS
CPCC Affiliate Professor: Michael Green
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Student Fellowship Recipient: Mahyar Kargar

1 Introduction

With increasing data rates and link distance in fiber-optic systems, the transmission path becomes severely limited by fiber non-idealities, especially dispersion. Intersymbol interference (ISI) is a fundamental limiting factor in band-limited communication links. In particular, multimode fiber links, which are the dominant fiber type in local area network (LAN) links like 10Gb/s Ethernet. Using adaptive equalizers is known to make the data communications over short ranges of the MMF possible. In this project a high-speed adaptive DFE is designed to combat the ISI caused by the band-limited MMF channel.

2 Summary of Accomplishments

The design of high speed delay cells, the slicer, D flip-flops and summing circuits have been completed.

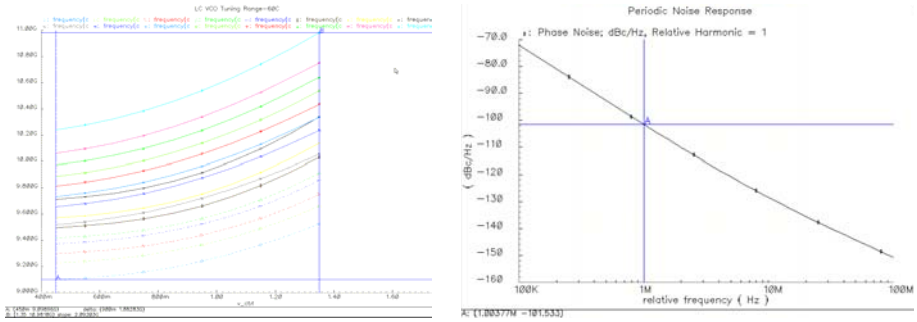
The 3-tap feedforward, 3-tap feedback DFE is simulated in Matlab for 10Gb/s PRBS-32 input. The channel model is taken from ModeSYS for 100m of 62.5μm MMF with 1310nm laser for over-field launching condition. The MMF model provided by ModeSYS, correlates well with the Cambridge model, MMF mode used in 10Gb/s Ethernet standard.

A 10GHz LC VCO with $\pm$ 10% tuning range is realized to be used in the CDR loop. The VCO tuning range and phase noise are shown in Fig. 1(a) and 1(b), respectively. The tuning range is from 9.09GHZ to 10.98GHz. The phase noise is -101.5dBc/Hz at 1MHz offset.

To get better performance for the high-speed blocks, the design is migrated to Jazz CA13 0.13μm CMOS design kit. The design of VCO, slicer, D flip-flops and the gain control loop is migrated and simulated in the new design kit. The design of CDR building blocks is also completed in CA13 design kit.

3 Ongoing Work

1. Migrating the remaining blocks to the CA13 design kit.
2. Completing the design of the adaptive DFE. A high-speed summing circuit using inductive peaking,needs to be realized.
3. Completing the design of the LMS circuit and verifying its convergence properties using transistor level simulations.
4. Top level simulation of the 10Gb/s CDR using Alexander phase detector.
5. Layout and post-layout extraction of the remaining blocks.



(a) (b)

Figure 1: 10GHZ *LC* VCO(a)Tuning range (b) Phase noise

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

CPCC Fellowship Spring Quarter, July 2007

Progress Report on Aggressive Power Management Utilizing Fault Tolerant Adaptation for Wireless Systems

Graduate Student: Amin Khajeh Djahromi
CPCC Affiliate Professor: Dr. Ahmed Eltawil

Project overview:

This project aims to utilize the algorithmic resilience to errors of certain systems such as communication and multimedia systems to minimize power consumption. This algorithmic resilience can be utilized and co-designed with the hardware circuitry in mind to provide protection not only to functional induced faults but also to hardware induced faults. Resilience to hardware-induced faults makes power reduction techniques such as aggressive Vdd scaling feasible, while increasing the effective yield of the chip via masking errors. By permitting the dynamic scaling of Vdd beyond the "safe" operating range, it is possible to reduce power further while still maintaining correct operation of the overall system

Progress:

The following describes our progress:

a) Identified memory failure statistics due to voltage scaling with process variations. Process variation leads to a uniform distribution of voltage scaling induced faults which is beneficial because it can be easily detected and corrected by subsequent system blocks such as convolution decoders in case of communication systems.
b) Built a complete simulation and analysis platform for simulating different memory architectures, including the effect of process variations. This work has resulted in a web based interface that will be available to the research community by Q4'07.
c) Performed experimental verification of the error distribution of voltage induced faults in collaboration with IBM. The test memory was a 38KB (512x76) 8T SRAM fabricated in 65nm technology. Figure 1 shows the distribution of faults across the test memory as a function of voltage. Note the uniform distribution of faults as the voltage is reduced. Figure 2 illustrates the probability of failure as a function of the overall chip voltage including the decoder and the sense amplifier.

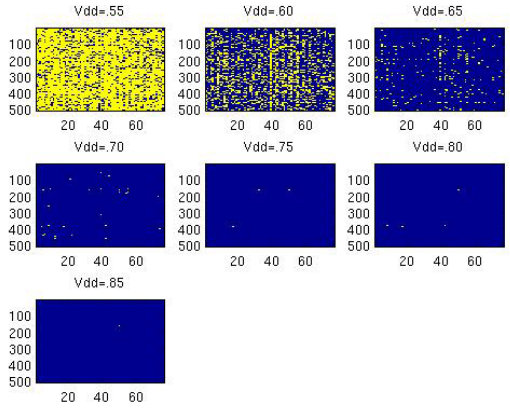


Figure 1 Fault distribution as a function of voltage

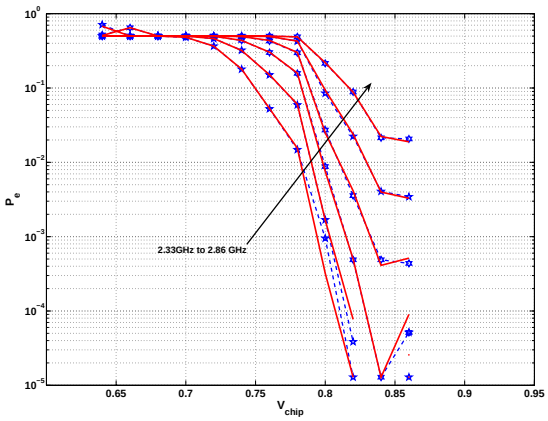


Figure 2 Probability of error as a function of the chip voltage.

Future Work:

In the future, we intend to focus on the following issues:

a) Creating a model of a communication system that encapsulates both the communication channel induced errors and the memory channel induced errors with the aim of creating a decoder that jointly protects against functional and hardware errors.
b) Researching statistical memory transistor sizing with the goal of finding the optimal sizing or circuit configuration for SRAM cells that simultaneously protects against process variation and allows for maximum voltage scaling thus achieving minimum energy consumption.

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

CPCC Fellowship Spring Quarter Progress Report, 2007

Project Name: 7 Transistor Fault Tolerant SRAM

Graduate Student: Mohammad A Makhzan, EECS (on CPCC Fellowship for SQ 2007)

CPCC Affiliate Professors: Fadi J. Kurdahi and Ahmed Eltawil.

Project Overview:

As technology proceed to sub 90 nm and smaller geometries, processing technology for compact SRAM memories faces new limitations. Sub wave length lithography and small geometry device variation such as random dopant fluctuation, channel length variation and line edge roughness enforce a larger distribution of threshold voltage (Vt) than before. Variation of Vt is followed by wider distribution of highest operable frequency. Designing for worse case which is the safest design leave us no choice but to limit our selves to the lowest part of frequency distribution curve which is not desirable. In Systems supporting Dynamic Voltage Scaling the effects of process variation will be more obvious in the circuit behavior further increasing the probability of cell failure. In this work we are designing a new fault tolerant memory cell consisted of 7 transistors and a capacitor which will lower the probability of cell failure, the new architecture lowers the read upset in an untraditional fashion (using the extra capacitor and the transistor) and allows designing the cell for faster access and writing time without a concern about increased read upset failure. In the result read upset failures, access failures and write failures which are the source of most SRAM failures will be addressed.

Progress:

The 7T SRAM was designed and tested for few corner cases. Using Hspice simulation we ran test cases for 180nm, 130nm nm technology using standard industry models and for 65nm and 32nm technology using Predictive Technology Models (PTM). The fault tolerant behavior of the circuit was verified. We are currently in the process of developing a layout, estimation of power consumption and developing the extra logic required for driving the extra RD (read signal) to the circuit.

Going forward we will simulate the new circuit to obtain the probability of the new cell failure when the voltage is scaled and compare it with the traditional 6T cell with the same size. The power consumption and areas overhead (and other trade offs) will be analyzed and studied. The new cell then will be used in constructing a new fault tolerant cache.

Publication:

(This publication is related to the project which started on spring 2006 and still continued. We are currently working on designing a low power wave pipelined fault tolerant cache.)

M. Makhzan A. Jahromi, A. Eltawil, F. Kurdahi, “Limits on Voltage Scaling for Low Power, High Speed Caches.” The 25th International Conference on Computer Design

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
CPCC Fellowship Spring Quarter Progress Report, Jun 2007

Project Name: **SOC Power Optimization Framework**
Graduate Student: **Sudeep Pasricha**, ICS (on CPCC Fellowship for SQ 2007)
CPCC Affiliate Professors: **Nikil D. Dutt** and **Fadi J. Kurdahi**

Project overview

The long term goal of the proposed project is to develop a system level methodology for power optimization for SoCs. In the immediate term, the proposed project will investigate techniques for efficient power modeling of SOC bus architectures, as well as of system-level IP blocks, and their use in the architectural exploration of IP-based SOC designs. On the basis of such power models of the system, we will be able to explore the architectural design space and evaluate various scheduling schemes. Meanwhile, the model is designed to be easily refined as the design process goes through the design flow, providing more accurate estimating of system performance and power consumption. The major purpose of the model is to provide a vehicle for researches on power optimization, such as the HAIM/DOSE (Hierarchically Abstracted IP modeling by Data Organization Space Exploration) exploration flow proposed earlier. The model and exploration flow are based on the COMMEX transaction-level communication architectural framework, on which we will study the H.264 application (the latest video coding standard), and JPEG2000 (the latest still image coding standard).

Progress

During Spring 07, we engaged three students in this project and made steady progress. The student supported on CPCC Fellowship was Sudeep Pasricha, who focused on power estimation for on-chip communication architectures, the overall SystemC modeling framework design as well as a case study of the H.264 decoder. Young-Hwan Park worked on gate-level power data extraction for communication architectures, developing ASIC power models and on the H.264 RTL integration effort. Kiarash Amiri was involved in processor modeling and software simulation. During the spring quarter, we accomplished the following:

- We continued our work investigating the impact of PVT (process, voltage and temperature) corners on power consumption at the System-on-Chip (SoC) level, especially for the on-chip communication infrastructure. We conducted several experiments to show how there are significant variations in power consumption across different corners for a given technology library. We showed how it is possible to "scale up" and abstract the PVT variability to characterize the true design space early on in the design flow, at the system level. We proposed scaling relations to quickly create power models for the different PVT corners, to estimate the power consumption of the bus matrix at the system level. The scaled power models took several orders of magnitude less time to create than the traditional macro-modeling approach, with a maximum absolute estimation error of 14%, which is extremely good for early power estimation at the system-level. Finally, we experimentally established the importance of considering PVT corners during system-level power exploration.
- Submitted a paper titled "Incorporating PVT Variations in System-level Power Exploration of On-Chip Communication Architectures" to the ICCAD conference.
- We developed a methodology to generate a hierarchy of power models for power estimation of custom hardware IP (ASIC) blocks, enabling a trade-off between power estimation accuracy, modeling effort and estimation speed. Our power estimation approach was shown to enable several novel system-level explorations -- such as observing the effect of clock gating, and the effects of tweaking application-level parameters on system power -- with an estimation accuracy that is close to the gate-level. We implemented our methodology on an H.264 video decoder prediction IP case study, created power models, and evaluated the effects of varying design parameters (e.g., clock gating, I/P ratios, Quantization), allowing rapid system-level power exploration of these design parameters.
- Submitted a paper titled "System Level Power Estimation Methodology with H.264 Decoder Prediction IP Case Study" to the ICCD conference.
- We continued work on processor modeling and power estimation for on-chip microprocessors.

- We continued our work on integrating the various components of the H.264 decoder at the RTL level with an AMBA AHB-based communication backbone.

Going forward, our goal in 2007 is to carry on our work dealing with exploration of system level power estimation for the different types of communication architectures, under process variations, as well as continue our work on power estimation of ASIC blocks. We plan to apply all our proposed methodologies to study system level power optimization techniques on the H.264 and JPEG2000 application drivers.

Publications

1. S. Pasricha, Y-H. Park, F. Kurdahi, N. Dutt, " Incorporating PVT Variations in System-level Power Exploration of On-Chip Communication Architectures ", ***submitted to International Conference on Computer-aided Design (ICCAD),*** **Apr 2007**
2. Y-H. Park, S. Pasricha, F. Kurdahi, N. Dutt, "System Level Power Estimation Methodology with H.264 Decoder Prediction IP Case Study ", ***submitted to International Conference on Computer Design (ICCD)*** **May 2007**

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

CPCC Fellowship Third Quarter Progress Report, July 2007

Project Name: Channel Estimation/Tracking in wireless systems using Affine Precoding

Graduate Student: Chitaranjan Pelur Sukumar
CPCC Affiliate Professor: Dr. Ahmed Eltawil

Project overview:

Recently, the advantages of using Channel State Information sent as feedback from the receiver to the transmitter has been studied extensively, specifically in the area of precoder design. However we believe that jointly designing the precoder and training matrices are the best way to achieve certain optimality criteria such as Capacity, Minimum Mean-Square-Error etc. This joint design will reveal the optimal power distribution between data and training symbols. We believe that by using the Kalman filtering framework to track channel changes, we can also derive the optimal power distribution in time.

Progress:

The following describes our progress:

a) All algorithms were modified to implement the conventional orthogonal training scheme, i.e. training and data symbols are assumed to be on different sub-carriers.
b) A constrained-frequency domain algorithm which specifies the power distribution between pilots and data to achieve minimum mean-square symbol error. This algorithm is extremely robust as it does not depend on various channel statistics. Noise due to channel estimation is also taken in consideration by the algorithms.
c) By assuming a Gauss-Markov model and also assuming that channel statistics are known, a constrained-frequency domain algorithm to implement the Kalman filter was formulated.

Future Work:

We are still working on:

a) Optimal power distribution to maximize capacity.
b) Optimal power distribution to maximize capacity and minimize mean square error in the Kalman filter algorithm.
c) Viability of the Kalman filter algorithm in the case when there is no feedback. After estimating the channel once, it might be possible to maintain the quality of the channel estimate in the mean square sense and still reduce the amount of power invested in training.

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
Graduate Fellowship - Progress Report for Spring Quarter 2007

Ph.D. Student: Hulya Seferoglu
Date: July 6, 2007
CPCC Affiliate Professor: Athina Markopoulou

Overview: During the spring quarter 2007, we continued our work on the problem of *video streaming over wireless using network coding* in several directions. We formulated a second network coding scheme for video, *NCVD*, to achieve further video quality improvement over *NCV,* which was proposed during winter 2007. We conducted extensive simulations for both NCV and NCVD and additional scenarios. We also analyzed the complexity of NCV and NCVD. We submitted a paper to the IEEE Packet Video Workshop'07 and archived a technical report on arXiv.org [1].

Network Coding for Video: Our work builds on the recent work by Katti et al. [5], which demonstrated that network coding can increase throughput over a broadcast medium, by mixing packets from different flows into a single packet, thus increasing the information content per transmission. Our key insight is that, when the transmitted flows are video streams, network codes should be selected so as to maximize not only the network throughput but also the video quality. During the winter quarter 2007, we proposed a video-aware opportunistic network coding scheme, *Network Coding for Video (NCV)*, that takes into account both (i) the decodability of network codes by several receivers and (ii) the importance and deadlines of video packets. During the spring quarter 2007, we finalized NCV and we also proposed a second coding scheme (*NCVD*) that uses not only the packet at the head of the queue, but also packets ``deeper'' in the queue, thus further improving the video quality.

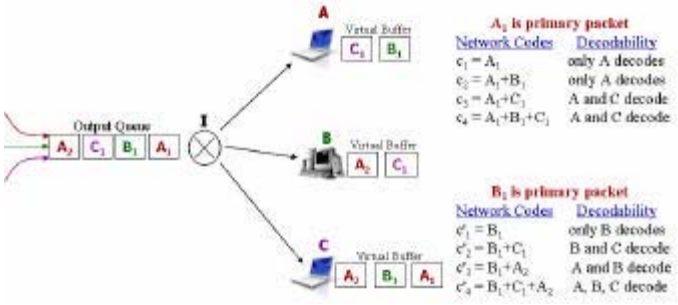


Figure 1: Example of NCVD

Example: Fig. 1 shows an example that illustrates the basic idea behind NCVD. (For clarity, we show and compare a scenario similar to the scenario used to illustrate NCV in the report for winter 2007). Node *I* is an access point in a WLAN or an intermediate node in a wireless mesh network, and *A*, *B*, and *C* are clients receiving video streams. *I* can transmit any combination of packets (using bitwise XOR to form a code) from its output queue. The code selection in NCV considers only the head-of-line packet in the output queue as a primary packet for the network code, and the other packets as possible side packets. This limits the candidate codes to those that are decodable together with this single primary packet. NCVD looks into the entire output queue and considers all active packets as candidates to be the primary packet, thus increasing the options for candidate. In the example of Fig. 1, one option is to select the head-of-line packet A_1 as the primary packet as in NCV. The best codes for this primary packet are c_2 or c_4. A different choice is to select B_1 as the primary packet, which leads to completely different set of candidate network codes. Code c'_1 achieves the maximum throughput improvement, and potentially the maximum video quality achievement, depending on the importance and urgency of all packets. This example demonstrates that increasing our options for the selection of primary packet expands the set of candidate codes, and thus can potentially improve both throughput and video quality.

NCVD Algorithm: More generally, NCVD constructs candidate codes c_k^i, $k = 1,2,...,2^{\Psi_m}$ for each candidate primary packet *(i)* in the output queue. Among all constructed codes, NCVD selects the code that maximizes the total impro vement in video quality for all clients:

$$\max_{p_i} \max_{k} (I_k^i)$$

where I_k^i is the total video quality i mprovement formulated as

$$I_k^i = \sum_{m=1}^{N} \sum_{l=1}^{L_k} (1 - e_l^k) \Delta_l^k g_l^k d_l^k$$

where: N is the number of clients, L_k is the number of the packets in the code c_k, e_l^k is the loss probability of packet l due to delay and/or channel errors, g_l^k is the indicator function for packet l being targeted to node m, and d_l^k is the indicator function for code c_k^i being decodable at node m. In every transmission opportunity, and among all possible network codes, c_k^i, the NCVD algorithm selects the primary packet and network code that maximize the total video quality improvement.

Complexity Analysis: Clearly, the performance improvements achieved by our schemes come at the cost of some additional complexity. Therefore, it became important to study the complexity of *NCV* and *NCVD*. We observed that the complexity of these algorithms comes from the code construction part and is specific to the network coding and not to the video-specific part of the problem. The bad news are that the problem at the heart of the code construction is an "independent set" problem, which is NP-complete but with efficient approximation algorithms known in the literature. The good news are that, in practice, the real-time delay requirements keep the buffers (and thus the number of packets considered in the construction of codes) small, thus significantly reducing the size of the problem which can be even solved by brute force enumeration.

Results: During the spring quarter, we used our simulator, developed in the winter quarter, to perform extensive simulations for both NCV and NCVD. We showed that NCV and NCVD provide significant quality improvement (up to 5 dB) for a wide range of simulation scenarios. The results from the perfomance evaluation of our schemes can be found in the technical report [1].

Ongoing Work: We consider extending our approach to: study additional topologies/scenarios, beyond the last-hop one-directional scenario; and extend the model to capture the dependency among video packets, the benefit of overheard packets and code selection across multiple time slots.

References:

[1] H. Seferoglu, A. Markopoulou, "Opportunistic Network Coding for Video Streaming over Wireless," *Technical Report arXiv:0706.1395v1 [cs.NI]*, June 2007.

[2] S. Katti, H. Rahul, W. Hu, D. Katabi, M. Medard, J. Crowcroft, "XORs in The Air: Practical Network Coding," *in Proc. of ACM SIGCOMM*, 2006.

Progress Report on MIMO Research: Spring 2007

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I. INTRODUCTION

Last quarter, we had mainly focused on codeword selection criterion assuming that there is already a given codebook. In this quarter, the goal was to design a limited feedback scheme for BICMB designing a codebook to quantize the channel state information.

II. CODEBOOK DESIGN

Our codebook design is based on generalized Lloyd's algorithm. We will minimize the average distortion

$$J = E\left[\min_{\hat{\mathbf{V}}_i \in \mathbb{V}} || \mathbf{V}\mathbf{D}^{opt} - \hat{\mathbf{V}}_i ||_F^2\right]$$

which is due to the optimal selection criterion analyzed last quarter and due to the nonuniqueness property of SVD. We assume that B bits are reserved for the limited feedback link to quantize the optimal beamforming matrix. In this algorithm, we will begin with an initial codebook of matrices $\tilde{\mathbb{V}}_0 = \{\tilde{\mathbf{V}}_{0,k}\}_{k=1}^{2^B}$ and iteratively improve it to generate a set of matrices $\tilde{\mathbb{V}}_m = \{\tilde{\mathbf{V}}_{m,k}\}_{k=1}^{2^B}$ until the algorithm converges. The algorithm can be summarized by the following steps:

1) Generate a large training set of channel matrices, $\mathbf{H}(n)$ and their corresponding right singular matrices $\mathbf{V}(n)$. Let Ψ be the set of all $\mathbf{V}(n)$s.

2) Generate an initial codebook of unitary matrices.

3) Set m = 1.

4) Partition the set of training matrices into $P = 2^B$ quantization regions where the k^{th} region is define as

$$\mathbb{X}_k = \{\mathbf{V} \in \Psi | \; || \mathbf{V}\mathbf{D}^{opt} - \tilde{\mathbf{V}}_{m-1,k} ||_F^2 \leq || \mathbf{V}\mathbf{D}^{opt} - \tilde{\mathbf{V}}_{m-1,l} ||_F^2 \;\; \forall \; k \neq l\}$$

5) Using the given partitions, construct a new codebook $\tilde{\mathbb{V}}_m$, with the k^{th} beamforming matrix being

$$\tilde{\mathbf{V}}_{m,k} = \underset{\hat{\mathbf{V}}:\; \hat{\mathbf{V}}^H\hat{\mathbf{V}} = \mathbf{I}}{\arg\min}\; E\left[|| \mathbf{V}\mathbf{D}^{opt} - \hat{\mathbf{V}} ||_F^2 \mid \mathbf{V} \in \mathbb{X}_k\right]$$

6) Define

$$J_m = \sum_{i=1}^{2^B} \sum_{n:\mathbf{V}(n) \to \tilde{\mathbf{V}}_{m,i}} || \mathbf{V}(n)\mathbf{D}^{opt} - \tilde{\mathbf{V}}_{m,i} ||_F^2$$

which is the average distortion.

The optimal solution of the optimization problem in step 5 gives the optimal centroid for the corresponding region. The distortion measure to be minimized can be rewritten as

$$\begin{aligned} || \mathbf{V}\mathbf{D}^{opt} - \hat{\mathbf{V}}_i ||_F^2 &= 2N - 2\mathrm{tr}\left[\Re[\hat{\mathbf{V}}^H\mathbf{V}\mathbf{D}^{opt}]\right] \\ &= 2N - 2\Re\left[\sum_{s=1}^{N} \hat{\mathbf{v}}_s^H \mathbf{v}_s e^{j\theta_s^{opt}}\right] \\ &= 2N - 2\sum_{s=1}^{N} |\hat{\mathbf{v}}_s^H \mathbf{v}_s| \end{aligned}$$

Therefore the original optimization problem can be rewritten as

$$\tilde{\mathbf{V}}_{m,k} = \underset{\hat{\mathbf{V}}:\; \hat{\mathbf{V}}^H\hat{\mathbf{V}} = \mathbf{I}}{\arg\max}\; E\left[\sum_{s=1}^{N} |\hat{\mathbf{v}}_s^H \mathbf{v}_s| \mid \mathbf{V} \in \mathbb{X}_k\right]$$

The maximization problem above does not have a tractable analytical solution. Next, we will modify the problem to find an approximate analytical solution. We will relax the unitary constraint and replace the constraint with having unit norm columns. In this case, the modified optimization problem is equivalent to finding independent optimal vectors which maximize each expectation. The individual maximization problem becomes

$$\tilde{\mathbf{e}}_{m,k}^{(i)} = \underset{\hat{\mathbf{e}}:\; ||\hat{\mathbf{e}}||_2^2 = 1}{\arg\max}\; E\left[|\hat{\mathbf{e}}^H \mathbf{v}_i| \mid \mathbf{v}_i \in \mathbb{X}_k^{(i)}\right] \quad i = 1, 2, \ldots, N$$

The optimal solution for the above problem can be found analytically as

$$\tilde{\mathbf{e}}_{m,k}^{(i)} = \text{ principal eigenvector of } E\left[\mathbf{v}_i\mathbf{v}_i^H | \; \mathbf{v}_i \in \mathbb{X}_k^{(i)}\right]$$

where numerical averaging is substituted for expectation during codebook design. Note that this matrix found by stacking the above solution as columns is not necessarily unitary; therefore to find the centroid we will utilize Euclidean projection to find the closest unitary matrix as follows

$$\tilde{\mathbf{V}}_{m,k} = \underset{\hat{\mathbf{V}}:\; \hat{\mathbf{V}}^H\hat{\mathbf{V}} = \mathbf{I}}{\arg\min} || \tilde{\mathbf{E}}_{m,k} - \hat{\mathbf{V}} ||_F^2$$

The closest unitary matrix can be found in closed form

$$\tilde{\mathbf{V}}_{m,k} = \tilde{\mathbf{U}}\tilde{\mathbf{W}}^H$$

where

$$\tilde{\mathbf{E}}_{m,k} = \tilde{\mathbf{U}}\tilde{\Sigma}\tilde{\mathbf{W}}^H.$$

Project name:	Cognitive Radio - Opportunistic and Reconfigurable Communication with Distributed Side Information
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Student:	Sudhir Srinivasa (sudhirs@uci.edu)
Date:	04 July 2007

Introduction:

Cognitive radio technology exploits overlay, underlay and interweave techniques to improve the utilization of the radio spectrum. Our work is primarily focused on the interweave interpretation of cognitive radio which dictates secondary transmissions only in frequency bands temporally unoccupied by the licensed users. Spectrum sharing between multiple secondary users and coexistence of multiple secondary systems are some of the challenges faced by multiuser cognitive radio networks.

Summary of Accomplishments:

Over the last quarter,two conference papers [1, 2] have been accepted at the IEEE Global Telecommunications Conference, 2007. We submitted one journal paper[3] associated with [2] and are working on a second journal paper[4] that builds on the ideas of [1].

In [3], we investigate the tradeoff between regulation and autonomy characteristic of cognitive radio systems with multiple secondary users. The main goal here is to identify the optimal number of secondary users that maximizes the sum throughput in the system under sensing constraints at the secondary users and interference tolerance constraints at the primary and secondary users. For the case of perfect sensing and zero interference tolerance, we find that neither pure autonomy nor pure regulation is throughput optimal. The optimal fraction of licensed users turns out to be very close to the duty cycle of the users. When the secondary users can vary their data transmission probabilities, we find that the optimal number of secondary users is very close to the average number of unoccupied slots. For the case of imperfect sensing and non-zero interference tolerance limits, numerical results exhibit an interplay between the tolerance of the primary users and the aggression of the secondary users. We find that the secondary users can exploit the tolerance of the primary users to transmit more aggressively, i.e., have a less sensitive primary user detector.

In [4], we consider a secondary system where the transmitter adapts its transmit power based on soft information provided by the spectrum sensor. We characterize the SNR and capacity optimal power adaptation strategies for both peak and average power constraints and with/without secondary channel knowledge at the secondary transmitter. We find that when the secondary channel knowledge is not available at the secondary transmitter, the optimal SNR power adaptation is binary for both peak and average transmit power constraints. We also provide numerical results for the SNR and capacity maximizing schemes for energy detection.

References:

[1] S. Srinivasa and S. A. Jafar, "*Soft Sensing and Optimal Power Control for Cognitive Radio*," Accepted for publication at the IEEE Global Communications Conference, 2007.

[2] S. Srinivasa and S. A. Jafar, "*Cognitive Radio Networks: How much Spectrum Sharing is Optimal?*," Accepted for publication at the IEEE Global Communications Conference, 2007.

[3] S. Srinivasa and S. A. Jafar, "*How much Spectrum Sharing is Optimal in Cognitive Radio Networks?*," Submitted to the IEEE Transactions on Wireless Communications.

[4] S. Srinivasa and S. A. Jafar, "*Soft Sensing and Optimal Power Control for Cognitive Radio*," In preparation, 2007.

Progress report on UWB research: Spring 2007

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***Abstract*—In the DS-UWB receiver, a pulse generator is needed to correlate the input pulse for synchronization. A flexible pulse generator was proposed and designed. In this pulse generator, a baseband gate pulse was generated with variable width and a frequency synthesizer was designed to provide dual carrier frequencies for upconversion.**

I. Introduction

In DS-UWB system [1], in order to avoid interference with available IEEE 802.11a system at 5GHz, the 7.5GHz bandwidth is divided into two bands: higher band (6GH~10GHz) and lower band (3GHz~5GHz). One challenge with the specification of spectrum in DS-UWB is to design a pulse signal which exactly has a dual band characteristic. Normally, current available designs [2] generate the pulse which only works on lower band, because of the difficulty to go higher band. In addition, most of the pulse generators are designed based on filtering a wideband signal. Therefore, they are not suitable for flexible design, which is another reason why only one band is chosen. In our previous work, a flexible pulse generator was designed and simulated to be suitable for both lower band and higher band separately. However, the delay in the divider causes problem for pulse alignment with generated carrier sine wave. Therefore, a revised version of the frequency synthesizer is proposed to solve this problem.

II. Method of Pulse Synthesis

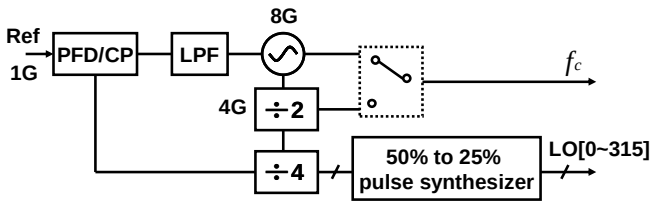

Fig. 1. Block diagram of pulse generator

To figure out the problem in the PLL, the previous frequency synthesizer is redrawn in Fig. 1, which includes 8GHz VCO, Injection Locking Frequency Divider (ILFD), CMOS static divider, conventional Frequency Phase Detector (FPD), Low Pass Filter (LPF) and a low-jitter Charge Pump (CP). In order to generate a pulse-like UWB signal, the 25% gate pulse baseband signal is mixed with a carrier sine wave to shift the pulse spectrum into a UWB specified spectrum. In a coherent UWB system, the pulse is required to have a constant phase to reduce the complexity for synchronization. Therefore, the phase difference between the gate pulse and the sine wave should be constant. The delay in each block in the frequency synthesizer can be well defined in system level. However, the delay due to circuit implementation is not easy controlled for signal at such a high frequency. To compensate for the delay caused by the divider and dead-zone in PFD, a variable phase shifter is added to the previous design.

Another concern is coming from the design in the synchronizer. In order to catch the short period from the longer input pulse strings, a two-step synchronization scheme – coarse acquisition and fine tracking was proposed. In the fine tracking block, a very accurate delay for a wideband pulse is needed. Since a cascade of such a delay stage is required in fine tracking, the required bandwidth is extremely high for current technology. Therefore, a pulse generator is required to provide the sine wave with five different phases for fine tracking. The revised pulse generator architecture is shown is Fig. 2.

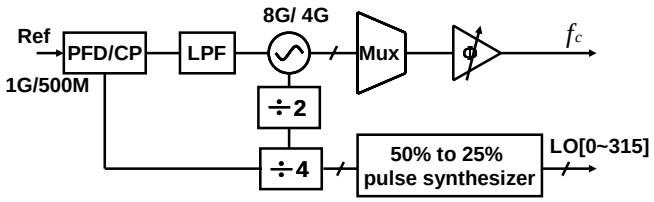

Fig. 2. Revised pulse generator block diagram

III. Progress and Future Plan

A new dual band frequency synthesizer for IR-UWB system is proposed and implemented in 0.13um CMOS process. Up to now, the whole synchronizer is ready and planned to tape out in two steps due to the heavy work. The first part, which is pulse generator, was taped out in July and the whole synchronizer, which includes pulse generator, coarse acquisition and fine tracking, will be taped out in August. The measurement will be done once the chip comes back in October.

References

[1] M. Z. Win and R. A. Scholtz, "Impulse radio: how it works," *IEEE Commun. Lett.*, vol. 2, no.2, pp. 36–38, Feb. 1998.

[2] T. Norimatsu *et al.*, "A novel UWB impulse-radio transmitter with all-digitally-controlled pulse generator," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2005, pp. 267-270.