UNIVERSITY OF CALIFORNIA
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CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

GRADUATE FELLOWSHIP PROJECTS PROGRESS REPORTS WINTER 2007

PROJECTS

ALPHABETIZED ACCORDING TO STUDENT LASTNAME

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GRADUATE FELLOWSHIP PROGRESS REPORT WINTER 07

Project Name: A Multi-Processor Architecture for Multimode Mobile Digital TV Platforms
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Introduction: As a base platform for NoC based system architecture, our NePA (*Ne*twork-based *P*rocessor *A*rray) [1] which are evolved from the previous MaRS (*Ma*cro-pipelined *R*econfigurable *S*ystem) will be used. Different from the original MaRS [2][2], the developed NoC architecture is applied and heterogeneous EU model which can be either programmable IPs or specific IPs is included. To support multiple standards in a single platform, the reconfigurability is an inevitable feature for the base platform.

Summary of Accomplishments: In the Winter Quarter 2007, as basic applications for benchmarking our NePA platform, the fast Fourier transform (FFT) was mapped onto our NePA. In order to map FFT kernels into homogeneous PEs, various parallelisms were observed. And finally we developed communication-optimized parallel FFT algorithm which is superior to previous parallel algorithms [3]. Specifically, by inventing a generic mapping scheme for communication, the amount of communication between each kernel can be minimized while the parallelism in FFT is fully utilized. With the developed parallel FFT algorithm, the unified kernel programming was performed and various simulations with different configurations of FFT algorithms were executed. By comparing the performance on commercial DSP processors such as TI C62x or C67x [4][5], we showed our proposed algorithm mapped in NePA platform outperforms in terms of cycle count for completing the given number of FFTs as shown in Figure 1 and Figure 2. On the other hand, with respect to the standardized criteria MFLOPS which represents the performance in the given operating clock frequency [6], our FFT algorithm on NePA has competitive or better performance in lower clock frequency, resulting in power saving. With this result, we submitted a paper to the conference [7].

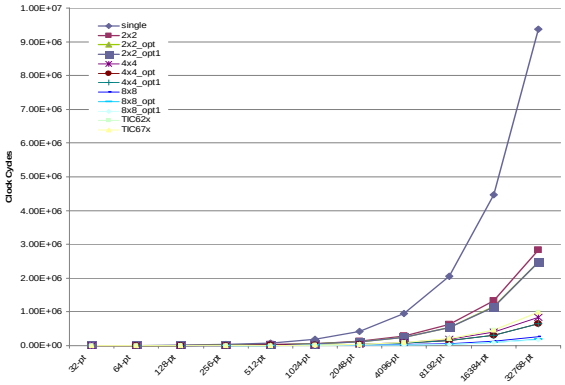

Figure 1. Comparison of cycle counts

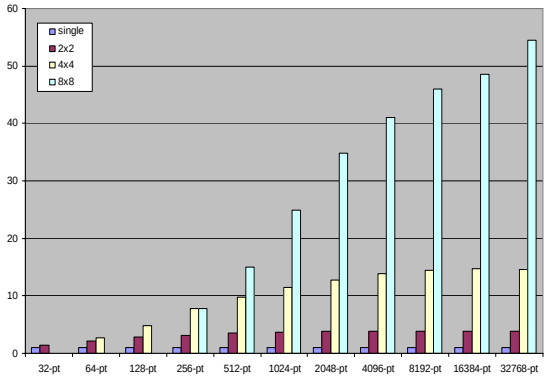

Figure 2. Comparison of performance gain

On going work: In order to show the versatility of our NePA platform, additional benchmarks with complicated algorithms such as LDPC, OFDM demodulation and so on, will be performed in homogeneous NePA platform. Also for heterogeneous NePA platform, our generic Network Interface (NI) should be refined to be fit in every different IPs attached to our NePA environment. Based on our previous definition of NI, some details of NI functionalities will be added.

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Misusing BitTorrent to Launch DDoS Attacks Progress Report - Winter 2007

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***Abstract*— Distributed Denial-of-Service (DDoS) attacks are a major problem in the Internet today. The typical mechanism to launch such attacks is to use worm compromised machines [1]. Another mechanism to launch DDoS attacks, which has received little attention, is to misdirect legitimate traffic from peer-to-peer systems toward a victim. Some studies have been conducted previously on systems such as Gnutella and Overnet. In recent years, peer-to-peer systems have evolved and new systems have been developed. We consider the most popular peer-to-peer system today, BitTorrent [2], and study how it could be used as a platform to launch DDoS attacks.**

I. Introduction

The battle between DDoS (and in general unwanted) traffic is an arm-race between defense and attack mechanisms. Both sides become increasing sophisticated and adapt to the adversary's choices. In the past, we focused on the defense side, particularly filtering mechanisms. During this quarter, we investigated the attacker's perspective, and identified some novel attack methods based on BitTorrent.

BitTorrent [2] is currently one of the most popular peer-to-peer (P2P) systems: its clients are widely spread all over the world and account for a large fraction of today's Internet traffic. During the winter quarter of 2007, we studied how BitTorrent can be exploited by misdirecting clients to send their traffic toward *any* host on the Internet. The volume of a BitTorrent swarm can thus be converted into firepower for launching a distributed denial-of-service (DDoS) attack that can exhaust the victim's resources, including access bandwidth and connection resources.

II. Contributions

Identifying Vulnerabilities in the BitTorrent Protocol. In this study, we have identified several novel vulnerabilities and exploits in the BitTorrent P2P system. These weaknesses can be exploited to launch a DDoS attack against any machine on the Internet.

Proof of Concept Implementation. To demonstrate that the identified vulnerabilities and exploits work, we have implemented them on open source BitTorrent software. We experimented with the developed exploits on the Internet and launched a small scale DDoS attack against our victim machine in Calit2. We analyzed the characteristics and effectiveness of such an attack.

Proposing Fixes. Finally, we proposed fixes to these vulnerabilities. We also contacted the organizations and individuals that run and implement BitTorrent - it ultimately lies in their hands to implement the fixes.

Constructing an Attack Model. Using the data/attack traces obtained from our Internet experiments, we started constructing a model that captures the spatial distribution of DDoS attacks. Such a model is missing from the literature and is important for testing proposed defense mechanisms.

III. Publication

The work during this quarter led to a workshop paper that will appear in USENIX SRUTI [3]. The interested reader is referred to the paper for details on the identified vulnerabilities, Internet experiments and measurements, and possible solutions. The paper is available online at our websites as well as at the workshop's website (*http://www.usenix.org/events/sruti07/*).

IV. Future Work

We continue this work in several directions. First, we are currently studying what the impact of a large scale DDoS attack using BitTorrent will be. Second, we are constructing an analytical model to describe the attack. Finally, we are using the data collected from this attack to test our optimal filtering mechanisms which we developed previously [4]. The data from this attack serves as a realistic scenario of a DDoS attack which is used as an input to our optimal filtering simulations.

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CPCC Progress Report, Winter 2007

Joint Source-Channel Coding and Quantized Feedback for Quasi-Static Fading Channels

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Our research is motivated by the recent demand for multimedia content delivery over wireless channels. Unlike data transmission systems where the objective is to minimize the bit errors, the design objective in multimedia transmission systems is to reduce the expected distortion of the received signal. In this context, the Shannon's separation theorem states that under an infinite block length assumption, the source and channel coding tasks can be performed separately. The latter assumption is easily violated in delay-sensitive and power-limited applications such as the case for slowly fading channels. Thus, we study joint source-channel coding approaches to this problem.

We consider a scenario where the delay constraint limits coding to a single block of fading. The reliable transmission rate, or the mutual information, then becomes a random variable and outage occurs if the transmission rate is larger than the mutual information. Our previous work considered a scenario where only the receiver has knowledge about the channel and time-sharing or superposition coding strategies were used to deal with the channel uncertainty [1], [2]. In our recent work, we have focused on the case where a noiseless feedback channel is available from the receiver to the transmitter. Assuming perfect channel knowledge at the receiver, the feedback channel is used to send a quantized version of the channel state information to the transmitter. The channel uncertainty is then reduced to a single quantization bin. We first derived a lower bound on the expected distortion assuming that the channel realization is known at the transmitter. We then proposed a low-complexity iterative algorithm based on dynamic programming and water-filling to numerically design the optimal channel quantizer and the power adaptation policy at the transmitter.

Figure 1 shows the results for a Rayleigh fading channel with single antennas at both the transmitter and the receiver. Figure 1(a) presents the results when power adaptation is not employed at the transmitter and Figure 1(b) shows the results with power adaptation. As we can see from the figures, a few bits of feedback (5 bits) achieve the performance lower bound and this justifies the quantization of the feedback information. Also show in the figure are the results for superposition coding with 1 and 5 layers [2]. We observe that in the high-SNR regime, superposition coding with 5 layers outperforms quantized feedback with 2 levels. This led us to investigate the asymptotic performance of the two schemes based on the distortion exponent that is defined as $\Delta = -\lim_{SNR\to\infty} \frac{\log \mathcal{E}_D}{\log SNR}$. We proved the following result in this context.

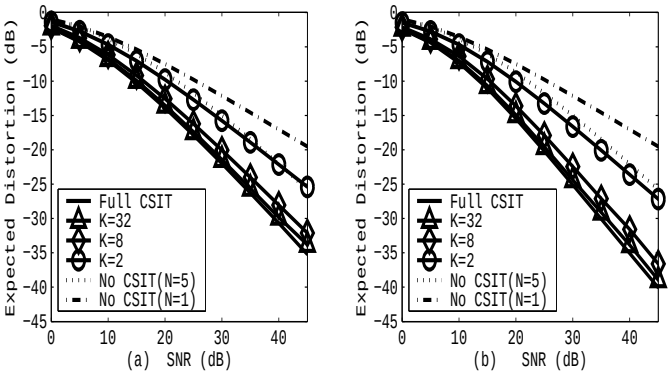

Fig. 1. Expected distortion for a SISO channel with $b = 1$ (a) Short-term power constraint (b) Long-term power constraint

Theorem: K-level noiseless feedback without power adaptation and K-layer superposition coding without feedback have the same distortion exponents.

Characterization of the distortion exponent with noiseless feedback and power adaptation is an ongoing effort. Moreover, in our future work we will also consider the effects of fading and a power-limited feedback link in a framework similar to [4].

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CPCC Fellowship Progress Report, Winter 2007:

Space-Time Block Coded Reconfigurable Multiple-Input Multiple-Output Systems

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I. Project Motivation and Overview

The principle by which reconfigurable antennas work is that by altering the antenna's physical configuration, we can control the current density on the antenna in a desirable manner and therefore change its radiation pattern/polarization/frequency. To change the antenna's physical configuration, one can use Microelectromechanical Systems (MEMS) switches or active devices such as diodes or field-effect transistors (FETs). By placing these components in strategic locations over the geometry of the antenna, the current paths can be engineered such that the resultant radiation patterns of the antenna follow some desired radiation requirements. Thus, one can create additional degrees of freedom in a communication system by intentionally changing the propagation characteristics of the channel.

In this project report, we present an open loop MIMO system using reconfigurable antennas at both the transmitter and the receiver. We show that the maximum achievable diversity gains in such a scenario are given by the product of the number of transmit and receive antennas and the number of reconfigurable states at the transmitter and the receiver. The motivation for this project is to introduce block coding schemes that are capable of extracting these additional degrees of freedom offered by employing reconfigurable antennas at the transmitter and the receiver.

II. Progress Report

During the course of this project, we first derive the code design criteria for a reconfigurable multi-element antenna (REMEA) system. We show that a REMIMO system employing N reconfigurable antennas at the transmitter with P radiation states and M reconfigurable antennas at the receiver with Q radiation states, is capable of providing a maximum diversity of $MNPQ$, therefore introducing a PQ fold increase in the diversity of the system. Furthermore, we use the generalization of QOSTBCs, introduced in [1], to design coding schemes for a reconfigurable MIMO communication system. The proposed coding scheme is capable of extracting the additional degrees of freedom offered by employing reconfigurable antennas at the transmitter and the receiver, for two transmit antennas and an arbitrary number of states. We perform the simulations for an open loop reconfigurable MIMO system, where the transmitter is a REMEA with $P = 2$ radiation states and the receive antennas are non-reconfigurable. In our simulations, we set $N = 2$ transmit antennas and $M = 1$ receive antenna. We consider two different antenna scenarios, one in which ideal reconfigurable antennas are used and a second scenario in which the correlation between radiation states is taken into consideration. Our proposed coding technique can achieve a diversity level of $MNP = 4$. The results are compared with the case where the transmit antennas are non-reconfigurable and a simple Alamouti scheme is used. We present both the 2×1 and 2×2 cases for comparison. Figure 1 depicts the bit-error-rate vs. SNR for 2 bits/sec/Hz using QPSK and an optimal rotation angle of $\pi/4$. As we notice from the figure, at a bit-error-rate of 10^{-3}, the performance of the new scheme in the ideal antenna scenario is about 3 dB better than the corresponding non-reconfigurable case, while correlation between states causes a performance degradation of about 0.5 dB compared to the ideal case.

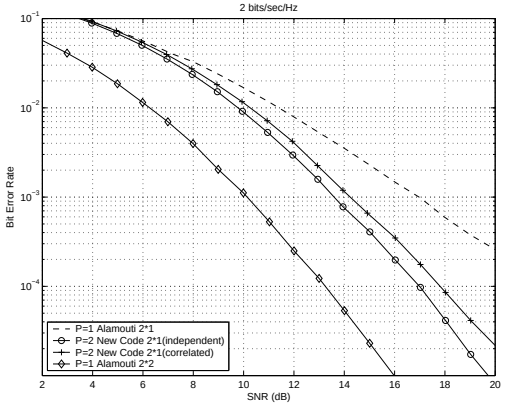

Fig. 1. BER vs. SNR for a remimo; 2 bits/sec/Hz using QPSK.

References

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Optimal Two-way Relaying with Half-duplex Relays

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I. Introduction

Cooperation and relaying in wireless networks offer enormous throughput enhancement by creating a virtual MIMO. However, one of the major limitations with relaying is the half duplex constraint at the relays, wherein the relays cannot transmit and receive simultaneously. This leads to a significant loss in spectral efficiency. Typically, for two hop relaying, the spectral efficiency loss is 50% compared to full duplex relaying [1]. Due to the broadcast nature of the wireless medium, Shannon's two way channel [2] where two users communicate to each other through a common channel, is well suited to wireless relay networks. Therefore, by employing two way relaying, the spectral efficiency loss due to half duplex constraint can be recovered to some extent.

II. System Model and Problem Statement

We consider a dual-source parallel relay network as shown in Fig. 1. In this model, two user nodes U_1 and U_2 wish to communicate to each other through a set of N half-duplex relays. Note that there is no direct link between the users. Here each source has power P_k, $k = 1, 2$ and the relays have

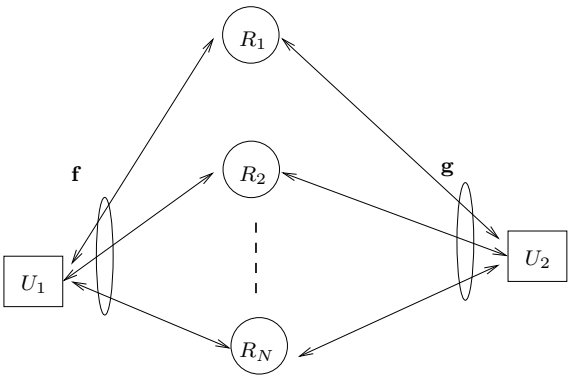

Fig. 1. Two-hop Two-way Parallel Relay Network

a sum power constraint of P_R. The $N \times 1$ vectors $\mathbf{f}$ and $\mathbf{g}$ represent the channels between the users and the relays. Due to the half-duplex nature of the relays, communication takes place in two slots. We assume quasi-static fading with global channel knowledge at all nodes. Further, we assume that the sources employ Gaussian signalling at their peak power. In the first time slot, the sources transmit x_1 and x_2 respectively. The relay received symbols during the first time slot are given by

$$\mathbf{r} = \mathbf{f}x_1 + \mathbf{g}x_2 + \mathbf{n_R} \tag{1}$$

where the elements of $\mathbf{n_R}$ are i.i.d. AWGN with unit variance. In the second slot, the relays amplify their received signal subject to the sum power constraint of the relays which is given by

$$\sum_{i=1}^{N} |d_i|^2(|f_i|^2P_1 + |g_i|^2P_2 + 1) = P_R \tag{2}$$

where $\mathbf{d} = [d_1 \ d_2 \cdots d_N]$ is the relay amplification vector. During the second slot, U_1 receives

$$y_1 = \left(\sum_{i=1}^{N} f_i^2 d_i\right) x_1 + \left(\sum_{i=1}^{N} f_i g_i d_i\right) x_2 + \sum_{i=1}^{N} f_i d_i n_{R_i} + n_{U_1} \tag{3}$$

As U_1 knows its transmitted symbol x_1, it can cancel out the terms associated with x_1 before decoding x_2. The received signal at U_2 is

$$y_2 = \left(\sum_{i=1}^{N} g_i f_i d_i\right) x_1 + \left(\sum_{i=1}^{N} g_i^2 d_i\right) x_2 + \sum_{i=1}^{N} g_i d_i n_{R_i} + n_{U_2}. \tag{4}$$

As before, x_2 can be canceled before decoding x_1. Therefore, for any relay amplification vector $\mathbf{d}$, the achievable rates are given by

$$R_1 = \log\left(1 + \frac{|\sum_{i=1}^{N} f_i g_i d_i|^2 P_1}{1 + \sum_{i=1}^{N} |d_i g_i|^2}\right) \tag{5}$$

$$R_2 = \log\left(1 + \frac{|\sum_{i=1}^{N} f_i g_i d_i|^2 P_2}{1 + \sum_{i=1}^{N} |d_i f_i|^2}\right). \tag{6}$$

We seek to determine the set of all possible achievable rates (R_1, R_2) that can be supported simultaneously under a sum power constraint at the relays.

Theorem 1: The relay amplification vector that maximizes any linear combination of rates $\mu_1 R_1 + \mu_2 R_2$ has the following structure.

$$d_i = \frac{\gamma f_i^* g_i^*}{D_1(i)\sin\theta + D_2(i)\cos\theta}, \qquad i = 1, 2...N \tag{7}$$

where

$$D_1(i) = \left(|f_i|^2P_1 + |g_i|^2(P_R + P_2) + 1\right)$$
$$D_2(i) = \left(|f_i|^2(P_1 + P_R) + |g_i|^2P_2 + 1\right)$$

and γ is necessary to satisfy the relay power constraint. ■

This result allows us to characterize all possible rate pairs that can be simultaneously supported. The resulting rate region is shown in Fig. 2. Here $\theta = 0$ maximizes the rate of User 1, while $\theta = \pi/2$ maximizes R_2. For all other linear combination of rates, θ takes a value from $[0, \pi/2]$. For the important case of sum rate $R_1 + R_2$, θ can be numerically optimized to

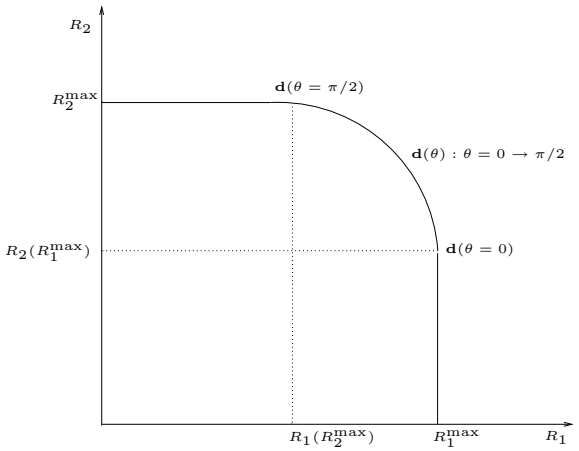

Fig. 2. Rate Region: Two-way parallel AF relay network

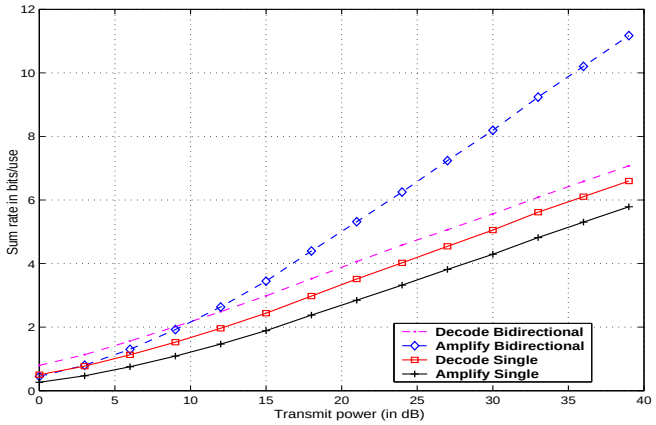

Fig. 3. Average rate of the two way channel in Fig. 1 as a function of transmit power $P_1 = P_2 = P_R$ for $N = 2$.

determine the optimal relay amplification factors. Notice that the N-dimensional relay optimization problem is reduced to a one dimensional optimization problem.

Fig. 3 shows the sum-rate of AF and DF for both one-way and two-way relaying as a function of transmit power of the nodes. For DF, we utilize the link scheduling model used in [3]. For the one way channel, DF is superior to AF. This is surprising as AF is more suited to parallel relay networks than DF. However, the link scheduling based DF outperforms AF due to the half duplex constraint of the relays. With AF, the destination requires two time slots to receive one symbol, i.e. only one hop is active at any time slot. However for the two-way channel, AF significantly outperforms DF. This is because two way relaying helps AF exploit both the hops efficiently. Here, each user receives one symbol in two time slots and thereby spectral efficiency is increased two-fold.

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CPCC 2006 Winter Quarter Report: Design of MEMS-reconfigurable decoupling networks for closely-spaced multi-element antennas in MIMO systems.

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I. Introduction

In today's wireless communication applications, compact and efficient antennas/arrays are required to satisfy the spacing requirements arising from multi-element antenna architectures (beamforming switching, multiple input multiple output, etc) and for integration purposes with other radio modules. Closely-spaced antennas suffer from mutual coupling which is a detrimental electromagnetic phenomenon that reduces the efficiency of the antennas. External decoupling networks can be used to compensate the mutual coupling among the antennas such that a good efficiency can be achieved over a reasonable frequency band.

As seen by the author, for a given antenna array geometry, the design of the decoupling networks is not unique. This opens the possibility to build MEMS-reconfigurable decoupling networks that while decoupling closely-spaced antennas, they are also simultaneously able to produce a set of uncorrelated radiation patterns/modes. This reconfigurable capability can be used in a MIMO [1] system to further enhance its performance.

II. Past Achievements (Fall Quarter)

During the fall quarter we developed a methodology for the design of specific decoupling networks for different antenna array topologies that are suitable to be made reconfigurable through MEMS technology. This methodology is based on the Generalized Takagi Decomposition of the measured Scattering Parameters matrices of the arrays. For the seek of knowledge, a Scattering Matrix is a matrix that relates the voltage wave incident on the ports to those reflected from the ports, and is normally measured directly with a vector network analyzer [2][3]. As shown by the authors, the Takagi factorization, provides a methodology to design decoupling networks that are reciprocal, that is, physically realizable, for any MEA structure. The multiplicity of the eigenvalues of the factorization is an indicator of the number of different decoupling networks that exist for a given array configuration.

III. Current Achievements (Winter Quarter)

During the winter quarter we concentrated our efforts on the physical implementation, with microstrip technology, of reconfigurable decoupling networks for circular arrays of closely-spaced antennas. In particular, we have finalized the design of a reconfigurable decoupling network for a circular array of two antennas and two distinct networks for a circular array of four antennas. The antennas are separated a distance of 0.14λ. We are currently conducting measurements on the radiation pattern and scattering parameters of the antenna array when connected to the proposed decoupling networks. Those measurements are obtained using the laboratory equipment, such as: HP 8510 2-50GHz network analyzer, and a conical compact anechoic chamber.

In particular for the circular array of two antennas, the resultant network uses one 180° hybrid followed by a switching network composed of several MEMS-switches, as shown in Fig. 1 and 2. Fig. 3 shows the scattering parameters at the output of the reconfigurable decoupling network. Notice that all the scattering parameters are below -15 dB, indicating that the antenna system is decoupled and matched, as desired. On the other hand, for the circular array of four antennas, one of the realized network designs uses four 180° hybrids, while a second network design uses three 180° hybrids. Both networks are followed by a switching network which is made out of several MEMS-switches. The switching networks are used to change the radiation state of the antenna array.

By means of combining the decoupling capabilities of the proposed networks with the reconfigurable capabilities introduced by the MEMS-switches, the resultant networks can be made to produce a set of orthogonal radiation patterns among its ports and among its different states. This is a novel capability that can be used to improve the performance of current MIMO systems. That is, the circular array of two antennas can therefore be seen as a single-port multi-antenna system that can radiate in two different states, where in each state the input port can be associated with a different orthogonal radiation pattern. Similarly, the four antennas circular array can be seen as a two-ports multi-antenna system that can radiate in two different states. Once again, the two different sets of radiation patterns, associated with the two input ports, are orthogonal among each other.

IV. Future work

Finally we will conduct system level simulations using MATLAB to find out the capacity and BER of the new

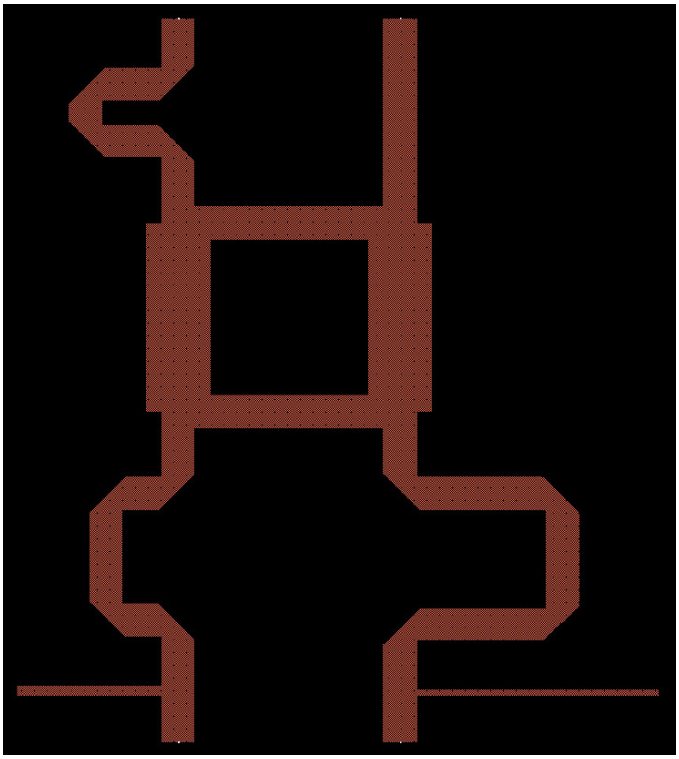

Fig. 1. Microstrip implementation of the decoupling network of the two antennas circular array generated using the Tagaki factorization.

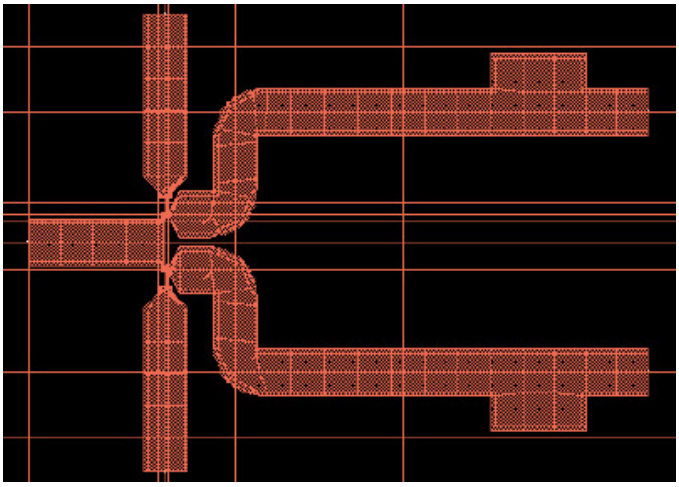

Fig. 2. Microstrip implementation of the switching network with four MEM switches on it.

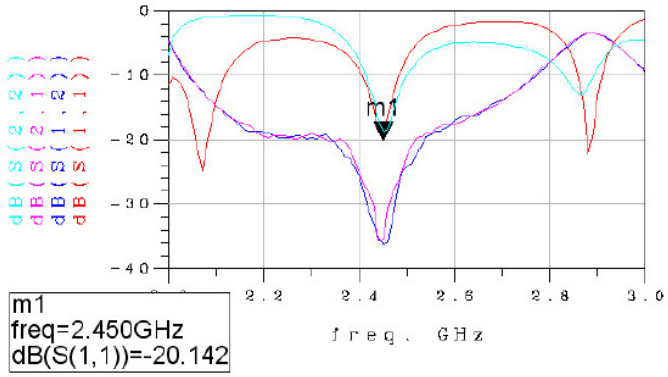

Fig. 3. Simulated scattering parameters at the output of the decoupling network for the two antennas circular array.

proposed system, as well as specific experiments to obtain the system capacity and diversity order of the proposed multi-antenna system, once fabricated.

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Modeling the 802.11e Enhanced Distributed Channel Access Function

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I. Introduction

The Enhanced Distributed Channel Access (EDCA) function of IEEE 802.11e standard [1] defines multiple Access Categories (AC) with AC-specific Contention Window (CW) sizes, Arbitration Interframe Space (AIFS) values, and Transmit Opportunity (TXOP) limits to support MAC-level Quality-of-Service (QoS). This quarter, we completed the design of an analytical model for the EDCA function which incorporates an accurate CW, AIFS, and TXOP differentiation at any traffic load [2]. The proposed model is also shown to capture the effect of MAC layer buffer size on the performance. Analytical and simulation results are compared to demonstrate the accuracy of the proposed approach for varying traffic loads, EDCA parameters, and MAC layer buffer space. In this report, we include a very short summary on the design of the model. The interested is referred to [2] for more details, explanations, and simulation results.

II. EDCA Discrete-Time Markov Chain Model

Assuming slot homogeneity, we propose a novel DTMC to model the behavior of the EDCA function of any AC at any load. The main contribution of this work is that the proposed model considers the effect of main EDCA QoS parameters (CW, AIFS, and TXOP) on the performance for the whole traffic load range from a lightly-loaded non-saturated channel to a heavily congested saturated medium. Although we assume constant probability of packet arrival per state (for the sake of simplicity, Poisson arrivals), we show that the model provides accurate performance analysis for a range of traffic types.

We model the MAC layer state of an AC$_i$, $0 \leq i \leq 3$, with a 3-dimensional Markov process, $(s_i(t), b_i(t), q_i(t))$. The definition of first two dimensions follow [3]. The stochastic process $s_i(t)$ represents the value of the backoff stage at time t. The stochastic process $b_i(t)$ represents the state of the backoff counter at time t. In order to enable the accurate non-saturated analysis considering EDCA TXOPs, we introduce another dimension which models the stochastic process $q_i(t)$ denoting the number of packets buffered for transmission at the MAC layer. Moreover, in our model, $b_i(t)$ does not only represent the value of the backoff counter, but also the number of transmissions carried out during the current EDCA TXOP (when the value of backoff counter is actually zero).

Using the assumption of independent and constant collision probability at an arbitrary backoff slot, the 3-dimensional process $(s_i(t), b_i(t), q_i(t))$ is represented as a DTMC with states (j, k, l) and index i. We define the limits on state variables as $0 \leq j \leq r_i - 1$, $-N_i \leq k \leq W_{i,j}$ and $0 \leq l \leq QS_i$. In these inequalities, we let r_i be the retransmission limit of a packet of AC$_i$; N_i be the maximum number of successful packet exchange sequences of AC$_i$ that can fit into one TXOP$_i$; $W_{i,j} = 2^{min(j,m_i)}(CW_{i,min}+1)-1$ be the CW size of AC$_i$ at the backoff stage j where $CW_{i,max} = 2^{m_i}(CW_{i,min}+1)-1$, $0 \leq m_i < r_i$; and QS_i be the maximum number of packets that can buffered at the MAC layer, i.e., MAC queue size. Moreover, a couple of restrictions apply to the state indices.

- When there are not any buffered packets at the AC queue, the EDCA function of the corresponding AC cannot be in a retransmitting state. Therefore, if $l = 0$, then $j = 0$ should hold. Such backoff states represent the postbackoff process [4],[1], therefore called as *postbackoff slots* in the sequel. The postbackoff procedure ensures that the transmitting station waits at least another backoff between successive TXOPs. Note that, when $l > 0$ and $k \geq 0$, these states are named *backoff slots*.
- The states with indices $-N_i \leq k \leq -1$ represent the negation of the number of packets that are successfully transmitted at the current TXOP rather than the value of the backoff counter (which is zero during a TXOP). For simplicity, in the design of the Markov chain, we introduced such states in the second dimension. Therefore, if $-N_i \leq k \leq -1$, we set $j = 0$.

Let p_{c_i} denote the average conditional probability that a packet from AC$_i$ experiences a collision. Let $p_{nt}(l', T|l)$ be the probability that there are l' packets in the MAC buffer at time $t + T$ given that there were l packets at t and no transmissions have been made during interval T. Similarly, let $p_{st}(l', T|l)$ be the probability that there are l' packets in the MAC buffer at time $t + T$ given that there were l packets at time t and a transmission has been made during interval T. Note that since we assume Poisson arrivals, the exponential interarrival distributions are independent, and p_{nt} and p_{st} only depend on the interval length T and are independent of time t. Then, the nonzero state transmission probabilities of the proposed Markov model for AC$_i$ are calculated as described in [2].

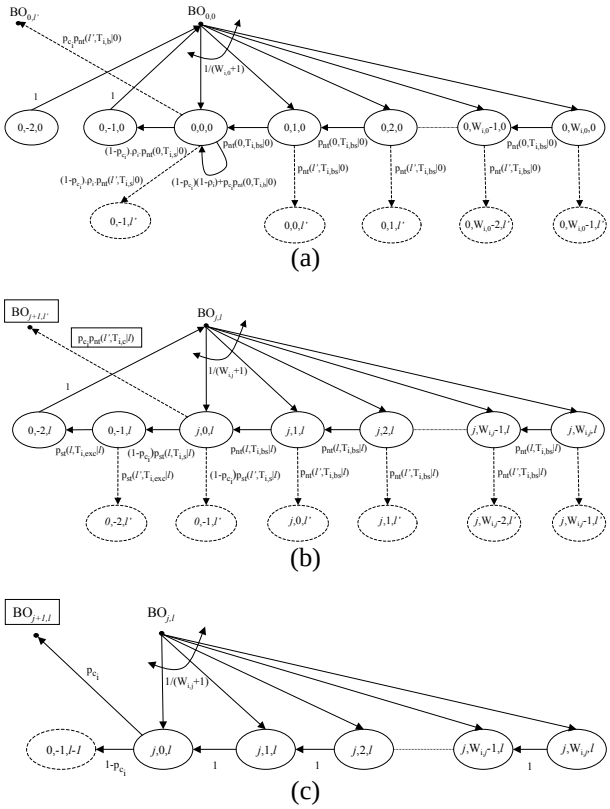

Fig. 1. Parts of the proposed DTMC model for N_i=2. The combination of these small chains for all j, k, l constitutes the proposed DTMC model. (a) $l = 0$. (b) $0 < l < QS_i$. (c) $l = QS_i$. Remarks: *i)* the transition probabilities and the states marked with rectangles differ when $j = r_i - 1$ (as as shown in [2]), *ii)* the limits for l' follow the rules in [2].

Parts of the proposed DTMC model are illustrated in Fig. 1 for an arbitrary AC_i with $N_i = 2$. The combination of these small chains for all j, k, l constitutes our DTMC model. In Fig. 1, let the time spent in a successful transmission be $T_{i,s}$ and a collision be $T_{i,c}$. Let $T_{i,bs}$ be the expected duration of a backoff slot, and let $T_{i,b}$ be the expected duration of a backoff slot given it is busy and one AC_i is in idle state. Let ρ_i be the probability that at least a packet arrival occurs in the current time slot for AC_i. We define $T_{i,exc}$ as the duration of a successful packet exchange sequence within a TXOP and $T_{i,txop}$ as the average duration of a TXOP for AC_i.

A. Steady-State Solution

Let $b_{i,j,k,l}$ be the steady-state probability of the state (j, k, l) of the proposed DTMC with index i. Let τ_i be the probability that an AC_i transmits at an arbitrary slot

$$\tau_i = \frac{\left(\sum_{j=0}^{r_i-1}\sum_{l=1}^{QS_i} b_{i,j,0,l}\right) + b_{i,0,0,0}\cdot\rho_i\cdot(1-p_{c_i})}{\sum_{j=0}^{r_i-1}\sum_{k=0}^{W_{i,j}}\sum_{l=0}^{QS_i} b_{i,j,k,l}}, \quad (1)$$

which implies, τ_i depends on p_{c_i}, $T_{i,bs}$, $T_{i,b}$, $T_{i,s}$, $T_{i,c}$, p_{nt}, p_{st}, and ρ_i. The non-linear system is solved using numerical methods [2].

B. Normalized Throughput Analysis

The normalized throughput of a given AC_i, S_i, is defined as the fraction of the time occupied by the successfully transmitted information. Then,

$$S_i = \frac{p_{s_i} N_{i,txop} T_{i,p}}{p_I T_{slot} + \sum_{i'} p_{s_{i'}} T_{i',txop} + (1 - p_I - \sum_{i'} p_{s_{i'}}) T_c} \quad (2)$$

where p_I is the probability of the channel being idle at a backoff slot, p_{s_i} is the conditional successful transmission probability of AC_i at a backoff slot, $N_{i,txop} = (T_{i,txop} - AIFS_i + SIFS)/T_{i,exc}$, $T_{i,p}$ be the average payload transmission time for AC_i, and T_{slot} is the duration of a time slot.

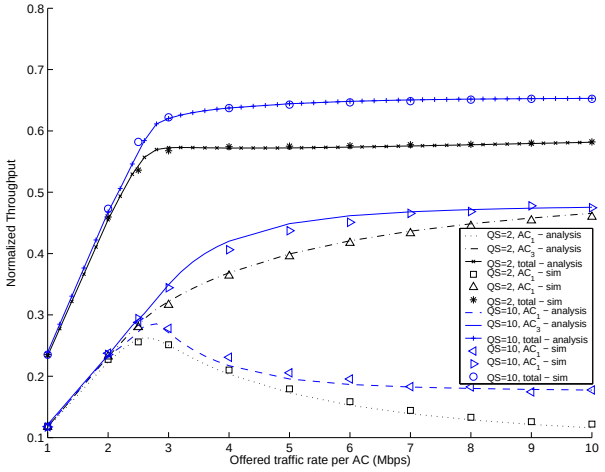

Fig. 2. Normalized throughput of each AC with respect to increasing load at each station.

III. Numerical and Simulation Results

We validate the accuracy of the numerical results by comparing them with the simulations results obtained from ns-2 [5]. For the simulations, we employ the 802.11e HCF MAC simulation model for ns-2.28 [6]. In simulations, we consider two ACs, one high priority and one low priority. Each station runs only one AC. Unless otherwise stated, the packets are generated according to a Poisson process with equal rate for both ACs. We set $AIFSN_1 = 3$, $AIFSN_3 = 2$, $CW_{1,min} = 15$, $CW_{3,min} = 7$, $TXOP_1 = 3.008$ ms, $TXOP_3 = 1.504$ ms, $m_1 = m_3 = 3$, $r_1 = r_3 = 7$. For both ACs, the payload size is 1034 bytes. The simulation results are reported for the wireless channel with no errors. All the stations use 54 Mbps and 6 Mbps as the data and basic rate respectively ($T_{slot} = 9\ \mu s$, $SIFS = 10\ \mu s$). The simulation runtime is 100 seconds.

In our first experiment, there are 5 stations for both ACs transmitting to an AP. Fig. 2 shows the normalized throughput per AC as well as the total system throughput for increasing offered load per AC. The analysis is carried out for maximum MAC buffer sizes of 2 packets and 10 packets. The results show that our model can accurately capture the linear relationship between throughput and offered load under low loads, the complex transition in throughput between under-loaded and saturation regimes, and the saturation throughput.The proposed model also captures the throughput variation with respect to the size of the MAC buffer.

Fig. 3 displays the differentiation of throughput when packet arrival rate is fixed to 2 Mbps per AC and the station number

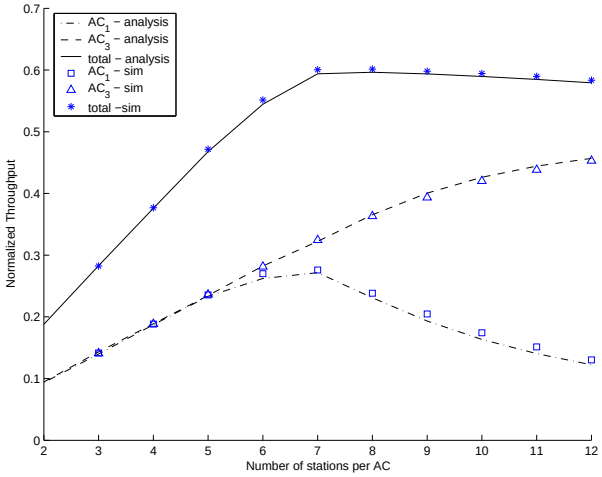

Fig. 3. Normalized throughput of each AC with respect to increasing number of stations when the total offered load per AC is 2 Mbps.

per AC is increased. We present the results for the MAC buffer size of 10 packets. The analytical and simulation results are well in accordance. As the traffic load increases, the differentiation in throughput between the ACs is observed.

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UC Irvine Center For Pervasive Communications and Computing Graduate Fellowship Progress Report Winter 2007

Project Name: Adaptive Equalization of Multimode Fiber Channels in 0.18μm CMOS
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1 Introduction

With increasing data rates and link distance in fiber-optic systems, the transmission path becomes severely limited by fiber non-idealities, especially dispersion. Intersymbol interference (ISI) is a fundamental limiting factor in band-limited communication links. In particular, multimode fiber links, which are the dominant fiber type in local area network (LAN) links like 10Gb/s Ethernet. Using adaptive equalizers is known to make the data communications over short ranges of the MMF possible. In this project a high-speed adaptive DFE is designed to combat the ISI caused by the band-limited MMF channel.

2 Summary of Accomplishments

The design of high speed delay cells, the slicer, D flip-flops and summing circuits have been completed.

The 3-tap feedforward, 3-tap feedback DFE is simulated in Matlab for 10Gb/s PRBS-32 input. The channel model is taken from ModeSYS for 100m of 62.5μm MMF with 1310nm laser for over-field launching condition. The MMF model provided by ModeSYS, correlates well with the Cambridge model, MMF mode used in 10Gb/s Ethernet standard. The DFE output eye diagram is shown in Fig. 1. The ISI is around 6ps.

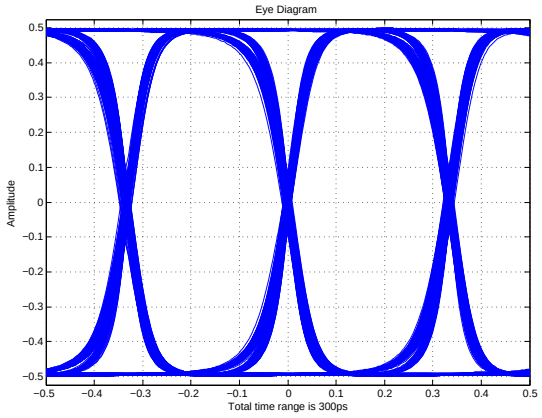

Figure 1: Simulated DFE output eye diagram

3 Ongoing Work

1. Completing the design of the adaptive DFE. A high-speed summing circuit using inductive peaking,needs to be realized.
2. Completing the design of the LMS circuit and verifying its convergence properties using transistor level simulations.
3. Design and top level simulation of the 10Gb/s CDR using Alexander phase detector.
4. Layout and post-layout extraction of the remaining blocks.

Progress Report on Aggressive Power Management Utilizing Fault Tolerant Adaptation for Wireless Systems: Winter 2007

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Abstract—**This report discusses how the cognitive radio concept can be extended to allow the system not only to manage shared resources such as spectrum, but to use this knowledge to optimize the overall system power consumption. We introduce a case study of video over wireless via a 3G WCDMA modem connected to an H.264 decoder. We show that by utilizing knowledge about the communication channel, a savings of more than 20% of the overall system power is possible while maintaining a required quality of service.**

I. Introduction

Cognitive radios (CR) running on programmable software defined radios (SDR) platforms have been under vigorous research since their introduction in the late 90s [1]. Even though the definition of CR might be different in different forums, most forums agree that the combination of SDR and CR provide the most flexible solution to support adaptive and intelligent communication systems. But by definition, a platform designed for general purpose processing cannot compete with a custom crafted ASIC from the power and area perspectives.

In this report, we intend to discuss novel methods of power management for cognitive radios that expand the concept of cognition to address jointly, both environment and self cognition with the target of minimum power consumption for a given set of conditions. This goal is achieved by dynamically managing not only the shared resources (spectrum) but also the hardware resources in terms of power consumption and subsequently increasing the battery life, while meeting the required system objective of reliable communication.

As mentioned in previous reports the algorithmic resilience to errors of the communication and multimedia systems can be utilized and co-designed with the hardware circuitry in mind to provide resilience not only to functional induced faults but also to hardware induced faults. In this report, we consider a case study of a hypothetical SDR platform performing video over wireless. Without loss of generality we consider a sample point where the modem is a 3G compliant WCDMA system, while the video decoder is an H.264 system. The most effective means of managing the power consumption of such a system is supply voltage scaling. In current techniques the operating voltage is conservatively chosen to guarantee 100% error free hardware. Our hypothesis postulates that by aggressively scaling the voltage even further and allowing a controlled amount of hardware errors to occur, an optimum operation point can be achieved whereas the algorithmic tolerance of the algorithms can be used to compensate for hardware failures while achieving a target performance metric such as bit error rate (BER, modem) or peak signal to noise ratio (PSNR, H.264). By knowing the statistics of the channel, one can decide on an optimum supply voltage for each section independently, where the error correction capabilities of each section will allow it to recover from hardware induced failures. For example, the channel coding of the modem offers resilience to errors while the error concealment algorithms in the H.264 decoder provides another layer of protection. Alternatively, one may decide to jointly change the supply voltage on both sections to achieve maximum power savings. The cognition cycle of the system thus becomes, observe the channel statistics, identify degrees of freedom to minimize power consumption (modem voltage scaling versus application voltage scaling), modulate operation conditions, and monitor performance metrics such as BER, PSNR.

II. Power Aware Designs

In general, hardware faults can be categorized into logic faults and memory faults. Tracking logic faults due to functional errors is an extremely difficult and currently unsolved problem. However, identifying memory faults presents a much more structured problem due to the structured nature of memories. In prior work [2], the authors have presented a complete analysis of memory faults under aggressive voltage scaling and methods of identifying and correcting for these faults in the context of wireless applications. This report builds upon these facts: a) A significant (sometimes even dominant) fraction of embedded metrics (power, performance, area) is related to memories which form a large portion of most modern communication transceivers. b) High percentage of the time, the receiver will be experiencing a relatively higher SNR than the minimum required for demodulation and the “slack” can be used to allow some limited and controllable errors to occur in the hardware to relax the circuit specifications. c) In the case of image/video system, filters can be used to reduce or even eliminate the effect of the hardware errors due to aggressive voltage reduction.

III. CASE STUDY

Based on the discussion in section II, we consider three cases as shown in figure 1.

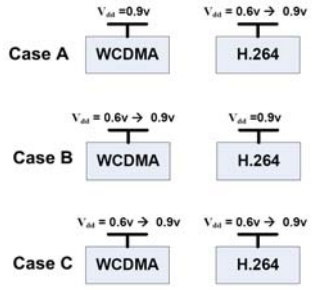


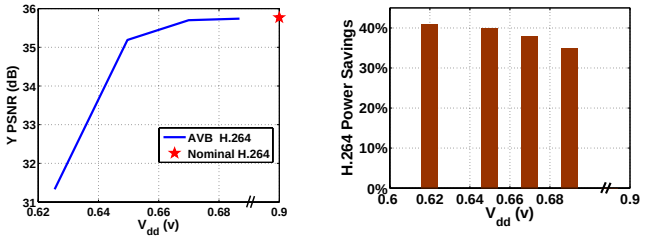
Fig.1. Three different cases that the radio can choose based on the operating conditions.

A. *Nominal WCDMA and Adaptive Voltage Biasing (AVB) H.264*

This case represents the scenario that WCDMA receiver does not benefit from a high received SNR. In other words, the received signal's SNR in modem is very close to the minimum required SNR and the WCDMA modem can not tolerate any error in its data buffering memories. Figure 2(a),(b) shows the results for this case.

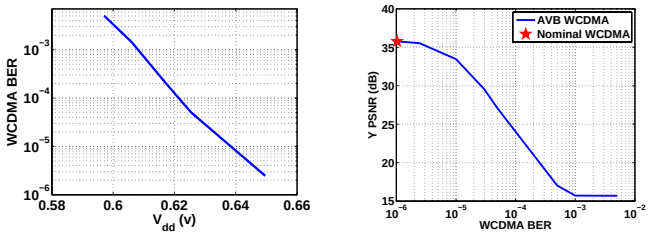
B. *Nominal H.264 and AVB WCDMA*

As previously mentioned in section II, a high percentage of the time the receiver will be experiencing a relatively higher SNR than the minimum required for demodulation. This slack" can be used to allow some limited and controllable errors to occur in data buffering memories by reducing memory voltage aggressively to lower the power consumption of the modem.



(a) (b)

Fig. 2. (a) Effect of AVB combined with filtering on H.264 decoder, (b) expected power saving by utilizing AVB for H.264 and post filtering.



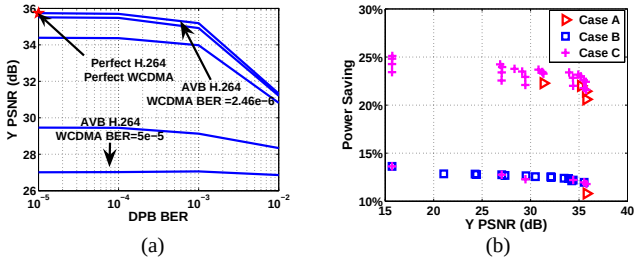
(a) (b)

Fig. 3. (a) Effect of aggressive voltage scaling on WCDMA BER, (b) Effect of WCDMA BER on Y PSNR of a perfect H.264 system.

Since the effect of the data stream out of the WCDMA receiver errors are dominant compared to the errors in the decoded picture buffer of H.264 on the output video quality, this case represent the scenario that the there is extra redundancy in the received signal that can be used to compensate for the effect of errors in the fault tolerant memories of the WCDMA modem. Figure 3(a),(b) shows the result for this case.

C. *AVB H.264 and AVB WCDMA*

This is the most general case where AVB is used on both the WCDMA receiver and the H.264 decoder. The assumption here is that the channel impairment is low and that it is possible to tolerate some minor degradation in the video output quality. There are, however some practical limitations to this approach. Figure 4(a) shows that the H.264 decoder can tolerate WCMA BERs between 10^{-6} to 10^{-5} and WCDMA BER of 10^{-5} or greater degrade the quality of video drastically. This fact points out the limitation on utilizing AVB for H.264 and WCDMA modem at the same time. In other words by setting the WCDMA voltage data buffering memories to a voltage that leads to error rate less than or close to 10^{-5} in WCDMA we can still benefit from utilizing AVB technique for the H.264 decoder. Figure 4(b) shows the power savings



(a) (b)

Fig. 4. (a) Utilizing AVB for H.264 and WCDMA , (b) Expected power savings for cases A, B and C .

that can be gained for three cases that we discussed above.

Based on this figure the radio can decide on the optimum approach for the desired Y PSNR and the corresponding power saving. In other words, for a fixed Y PSNR the system will decide on the approach that results in the maximum power saving. From the graph, we observe that some points are inferior to others. In other words, one case may yield higher power savings than another for the same target PSNR. Such points are considered as *pareto-optimal*. Case B points appear to be inferior to cases A and C. However, this is a direct conclusion of the ratio of power consumptions of the receiver and video decoder. Since the receiver consumes more than 3x the power of the H.264 decoder, one would expect to get more power reduction by AVB of the receiver. This situation would be reversed in another system where the ratios are the opposite. As expected, case C yields the most pareto-optimal design points since it is a superset of cases A and B.

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UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

CPCC Fellowship Winter Quarter Progress Report, 2007

Project Name: A New Fault Tolerant Architecture to scope with process Variation

Graduate Student: Mohammad A Makhzan, EECS (on CPCC Fellowship for SQ 2007)

CPCC Affiliate Professors: Fadi J. Kurdahi and Ahmed Eltawil.

Project Overview:

As technology scales to smaller geometries manufacturing laboratories face new limitations. Sub wave length lithography and small geometry device variation such as random dopant fluctuation, channel length variation and line edge roughness enforce a larger distribution of threshold voltage (Vt) than before. Variation of Vt is followed by wider distribution of highest operable frequency. Leakage also has a high dependency on Vt. Therefore large variation in the leakage in the result of process variation will be seen. On the other hand in larger technologies (90 nm and above) the dynamic power consumption was responsible for most of the circuit power consumption. Moving to smaller technologies leakage start becoming more of a concern as it become the main source of power consumption specially in 32 nm and below. But leakage is also strongly related to the supply voltage. By reducing the supply voltage leakage will decrease exponentially. The problem with decreasing the supply voltage is increased probability of failures in the logic and memory. In this work we are designing a new fault tolerant cache which handles a very large number of defects with very small effect on performance allowing the supply voltage to be scaled down. The new architecture although uses extra logic, but has lower power consumption since only a few small logical and memory circuits are operating at full supply voltage when all other parts will be voltage scaled.

Progress:

We modeled the architecture and tested it using a trace driven cache simulator. (DineroIV). We designed a small associative cache (IDC), an off cache defect map (BLB), a defect map buffer, replacement and finally mapping algorithms. The limits of lowering voltage on both memory and logic part of the cache memory for a 3 stage pipelined cache was studied. The modeled architecture (Enhanced DineroIV) was enriched by book keeping code to calculate the power consumption per instruction execution. Area over head for this design for our designed 16KB L1 cache is about 11% for 45nm technology and 12% for 32 nm technology. The average power saving across all benchmarks for 45nm technology was about 12.8% and for 32nm technology was about 46.3% compared to a traditional 16KB cache working at full Vdd.

Work in Progress:

The current design model a 3 stage pipelined cache. Going forward we are looking into introducing the same concepts into wave pipelined caches. We are considering to model the new architecture in SimpleScalar.

Publication:

(This is a publication from work that started on fall 2006 on fault tolerant JPEG 2000)

Mohammad A. Makhzan, Amin Jahromi, Ahmed Eltawil, Fadi Kurdahi, "A Low Power JPEG2000 Encoder with an Iterative and Fault Tolerant Error Concealment"

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
CPCC Fellowship Winter Quarter Progress Report, Apr 2007

Project Name: **SOC Power Optimization Framework**
Graduate Student: **Sudeep Pasricha**, ICS (on CPCC Fellowship for WQ 2007)
CPCC Affiliate Professors: **Nikil D. Dutt** and **Fadi J. Kurdahi**

Project overview

The long term goal of the proposed project is to develop a system level methodology for power optimization for SoCs. In the immediate term, the proposed project will investigate techniques for efficient power modeling of SOC bus architectures, as well as of system-level IP blocks, and their use in the architectural exploration of IP-based SOC designs. On the basis of such power models of the system, we will be able to explore the architectural design space and evaluate various scheduling schemes. Meanwhile, the model is designed to be easily refined as the design process goes through the design flow, providing more accurate estimating of system performance and power consumption. The major purpose of the model is to provide a vehicle for researches on power optimization, such as the HAIM/DOSE (Hierarchically Abstracted IP modeling by Data Organization Space Exploration) exploration flow proposed earlier. The model and exploration flow are based on the COMMEX transaction-level communication architectural framework, on which we will study the H.264 application (the latest video coding standard), and JPEG2000 (the latest still image coding standard).

Progress

During Winter 07, we engaged three students in this project and made steady progress. The student supported on CPCC Fellowship was Sudeep Pasricha, who focused on power estimation for on-chip communication architectures, the overall SystemC modeling framework design as well as a case study of the H.264 decoder. Young-Hwan Park worked on gate-level power data extraction for communication architectures, and the H.264 RTL integration effort. Kiarash Amiri was involved in processor modeling and software simulation. During the winter quarter, we accomplished the following:

- We investigated the impact of PVT (process, voltage and temperature) corners on power consumption at the System-on-Chip (SoC) level, especially for the on-chip communication infrastructure. With the shift towards deep sub-micron (DSM) technologies, the increase in leakage power and the adoption of power-aware design methodologies have resulted in potentially significant variations in power consumption under different PVT corners. Given a target technology library, we showed that it is possible to "scale up" and abstract the PVT variability at the system level, allowing characterization of the PVT-aware design space early in the design flow. We conducted several experiments to estimate power for PVT corner cases, at the gate-level, as well as at the higher system-level. Our preliminary results are very interesting and indicate that: (i) there are significant variations in power consumption across PVT corners, and (ii) the PVT-aware power estimation problem may be amenable to a reasonably simple abstraction at the system-level.
- We continued work on developing power estimation schemes for hardware ASIC blocks early in the design flow, at the system level. We proposed a hierarchical power modeling strategy to estimate power for ASIC blocks with varying accuracy, and experimented with applying these strategies to the H.264 decoder.
- We continued work on processor modeling and power estimation for on-chip microprocessors.
- We continued our work on integrating the various components of the H.264 decoder at the RTL level with an AMBA AHB-based communication backbone.

Going forward, our goal in 2007 is to carry on our work dealing with exploration of system level power estimation for the communication architectures, under process variations, which is an extremely important problem facing designers today. We are also actively focusing our efforts on developing power estimation models for other components such as memories, processors and ASIC blocks. We have begun work on power estimation of

ASIC blocks, and we intend to focus on this problem over the next few months. We plan to apply our methodologies to study system level power optimization techniques on the H.264 and JPEG2000 application drivers.

Publications

1. S. Pasricha, N. Dutt, "A Framework for Co-synthesis of Memory and Communication Architectures for MPSoC", ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol. 26, No. 3, pp. 408-420,*** **March 2007**
2. C. Shin, P. Grun, N. Romdhane, C. Lennard, G. Madl, S. Pasricha, N. Dutt, M. Noll, "Enabling Heterogeneous Cycle-Based and Event-Driven Simulation in a SPIRIT-Enabled Design Flow", ***Kluwer Journal on Design Automation of Embedded Systems (DAES),*** **Feb 2007**

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING

CPCC Fellowship Second Quarter Progress Report, May 2007

Project Name: Channel Estimation/Tracking in wireless systems using Affine Precoding

Graduate Student: Chitaranjan Pelur Sukumar
CPCC Affiliate Professor: Dr. Ahmed Eltawil

Project overview:

Channel estimation algorithms are extensively used in communication systems. However we believe that once a channel has been estimated, tracking the changes in the fading channel, instead of re-estimating it, will reduce the amount of power invested in training. After some initial studies, Kalman filter theory was found to describe a practical method to perform channel tracking. It also sets up a framework which enables us to find the optimum power distribution and placement of training and data symbols over time and frequency. This will be attempted for two possible scenarios: a) When no Channel State Information (CSI) is available at the transmitter and b) When feedback is present and receiver channel estimates are available to the transmitter. As the computational complexity of these algorithms is relatively high, we will formulate a sub-optimal but significantly simpler-to-implement constrained frequency domain algorithm.

Progress:

The following describes our progress:

a) A Kalman filter which is capable of estimating as well as tracking the channel. This Kalman filter in its most general form incorporates interference from the data when channel estimation is performed. When symbol estimation is performed, noise due to incorrect channel estimation is also factored in.
b) Cramer Rao Bound for the channel estimator has been found and the optimality condition for the best channel estimate for a given training power has also been determined.
c) We have a constrained-frequency domain algorithm which makes the complicated Kalman filter equations less computationally expensive to implement.

Future Work:

In the future, we intend to focus on the following issues:

a) Optimal power allocation and placement of pilots in the case without feedback. After estimating the channel once, we will determine if it is possible to maintain he quality of the channel estimate (MSE sense) in time by reducing the power in the training symbols. This will obviously enable us to drop our total transmitted power.
b) Joint Optimization of Precoder and Training matrices to meet certain optimality criteria (maximizing information rate, minimizing mean square error for the symbol estimate, maximizing SNR for ZF receiver, etc.) when Channel State Information (CSI) is available to the transmitter via feedback.

UC IRVINE CENTER FOR PERVASIVE COMMUNICATIONS AND COMPUTING
Graduate Fellowship - Progress Report for Winter 2007

Ph.D. Student: Hulya Seferoglu
Date: May 24, 2007
CPCC Affiliate Professor: Athina Markopoulou

Overview: During winter 2007, we focused on one of the problems that we identified during fall 2006, namely *video streaming over wireless using network coding*. We formulated the optimization problem, designed the first coding algorithm, developed a simulation setup and obtained preliminary results. This work, together with the follow-up work in spring 2007 led to the submission of a conference paper (in the spring quarter).

Network Coding for Video: Network coding is an emerging area [1] that started with [2, 3] in the context of multicast networks, stating that if intermediate nodes are allowed to perform simple operations on incoming packets, then the network can achieve the min-cut throughput to each receiver. Recently, the networking community has started to apply ideas from network coding to selected practical problems, such as peer-to-peer networks and wireless networks. Of particular interest to our work is [4], which demonstrated that network coding can increase throughput over a broadcast medium, by mixing packets from different flows into a single packet, thus increasing the information content per transmission. The work in [4] was tuned for data/TCP applications. Our key insight in this project is that, when the transmitted flows are video streams, network codes should be selected so as to maximize not only the network throughput but also the video quality. During the winter quarter 2007, we developed a video-aware opportunistic network coding scheme, *Network Coding for Video (NCV)*, that takes into account both (i) the decodability of network codes by several receivers and (ii) the importance and deadlines of video packets.

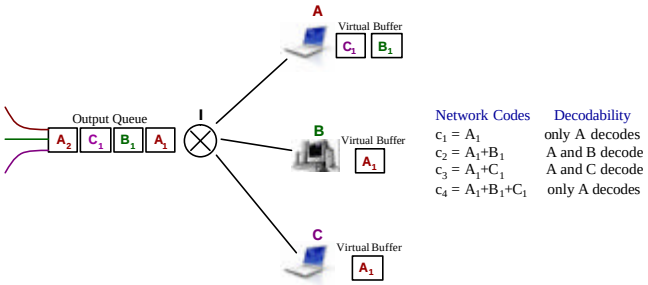

Figure 1: Example of Network Coding for Video (NCV)

Example: Fig. 1 shows an illustrative example. Node *I* is an access point in a WLAN or an intermediate node in a wireless mesh network, and *A*, *B*, and *C* are clients receiving video streams. *I* can transmit any combination of packets (using bitwise XOR to form a code) from its output queue. The selection of code in [4] considers the ability of the clients to decode the code, which in turn depends on packets previously received and overheard by the clients. In the example of Fig.1, it is obvious that c_2 and c_3 are the best network codes in terms of throughput: each transfers two packets to two clients. However, their throughput improvement is exactly the same: [4] would not differentiate among these codes and *I* would randomly select and transmit any of the two. Our key observation is that the selection of network code affects video quality and preference should be given to codes that consist of important packets in terms of distortion and urgency.

NCV Algorithm: We propose an algorithm that selects the best network code for video quality improvement, without compromising the throughput benefits of [4]. The outline of the algorithm is as follows. The first active (i.e. not transmitted within the last RTT) packet in the output queue is selected as a primary packet to be included in the network code. Additional side packets are selected and XOR-

ed together with the primary packet (i), to form the network code (c_k^i), so as to maximize the total video quality improvement (I_k^i) to all clients:

$$I_k^i = \sum_{m=1}^{N} \sum_{l=1}^{L_k} (1 - e_l^k) \Delta_l^k g_l^k d_l^k$$

where: N is the number of clients, L_k is the number of the packets in the code c_k, e_l^k is the loss probability of packet l due to delay and/or channel errors, g_l^k is the indicator function for packet l being targeted to node m, and d_l^k is the indicator function for code c_k^i being decodable at node m. In every transmission opportunity, and among all possible network codes c_k^i, the NCV algorithm selects the network code that maximizes the total video quality improvement for primary packet i:

$$\max_k I_k^i$$

Simulation Setup: During the winter quarter, we also developed a simulator from scratch to evaluate the effectiveness of NCV. Preliminary simulation results are encouraging: NCV provides significant quality improvement (up to 5dB) for scenarios based on Fig.1.

Ongoing Work: During spring 2007, we continue this work in several directions. We are developing a second network coding scheme for video, NCVD, to achieve further video quality improvement. We are conducting extensive simulations for both algorithms and additional scenarios. We are also exploring complexity issues and suboptimal algorithms.

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Progress Report on MIMO Research: Winter 2007

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I. Introduction

It has been shown [1] that it is possible to achieve full spatial diversity of NM independent of the number of streams $1 \leq S \leq \min(N, M)$ transmitted over quasi-static Rayleigh flat fading channels. This system is known as bit-interleaved coded multiple beamforming (BICMB). Design criteria for the interleaver and the convolutional encoder which guarantee full diversity and full spatial multiplexing is provided in [1]. In general, BICMB requires perfect knowledge of only channel eigenvectors at the transmitter, i.e., does not need the channel gains (eigenvalues) at the transmitter.

In this quarter, the goal was to design a limited feedback scheme for BICMB. We mainly focused on codeword selection criterion assuming that there is already a given codebook. We provide an optimal Euclidean distortion measure for the selection of the best precoder from the codebook due to the non-uniqueness property of SVD [2].

II. Main Result

We assume that there exists a codebook and we wish to find a criterion to choose the best approximation to $\mathbf{V}$ from the codebook $\mathbb{V} = \{\hat{\mathbf{V}}_i\}_{i=1}^{C}$, where C is the codebook size.

Selection Criterion - Euclidean (SC-E) : The receiver selects $\mathbf{V}_L$ such that

$$\mathbf{V}_L = \underset{\hat{\mathbf{V}}_i \in \mathbb{V}}{\arg\min} \mid\mid \mathbf{V} - \hat{\mathbf{V}}_i \mid\mid_F^2. \tag{1}$$

This selection criterion aims to find the codebook element closest to the optimal beamforming matrix $\mathbf{V}$. It can be argued that this criterion asymptotically diagonalizes the system as the number of feedback bits goes to infinity.

However, the nonuniqueness property of SVD makes straightforward application of (1) nonpractical. Assume that an application of SVD for a given instantiation of the $\mathbf{H}$ matrix yields a $\mathbf{V}$ matrix. Assume that when $\mathbf{V}$ is multiplied by all diagonal unitary matrices $\mathbf{D}$, one gets the set $\mathbb{S}_{\mathbf{V}}$. It should be clear that the closest member of $\mathbb{V}$ to $\mathbf{V}$ is not necessarily the closest member of $\mathbb{V}$ to $\mathbb{S}_{\mathbf{V}}$. As a result, one needs to modify (1) such that the minimum distance between two sets $\mathbb{V}$ and $\mathbb{S}_{\mathbf{V}}$ can be calculated. A way to accomplish this is

$$\mathbf{V}_L = \underset{\hat{\mathbf{V}}_i \in \mathbb{V}, \mathbf{D} \in \mathbb{D}}{\arg\min} \mid\mid \mathbf{VD} - \hat{\mathbf{V}}_i \mid\mid_F^2 \tag{2}$$

where $\mathbb{D}$ stands for the set of all *diagonal unitary* matrices.

Proposition 1: The minimization in (2) is equivalent to the following minimization problem

$$\mathbf{V}_L = \underset{\hat{\mathbf{V}}_i \in \mathbb{V}}{\arg\min} \mid\mid \mathbf{VD}^{opt} - \hat{\mathbf{V}}_i \mid\mid_F^2. \tag{3}$$

The k^{th} diagonal element of $\mathbf{D}^{opt}$ is given as

$$\theta_k^{opt} = -\phi_k \qquad k = 1, 2, \ldots, S \tag{4}$$

where $0 \leq \phi_k < 2\pi$ is the phase of $\hat{\mathbf{v}}_{ik}^H \mathbf{v}_k$. The vectors $\hat{\mathbf{v}}_{ik}$ and $\mathbf{v}_k$ correspond to the k^{th} column of $\hat{\mathbf{V}}_i$ and $\mathbf{V}$, respectively.

Proof: Without loss of generality, let $N \leq M$ and $S = N$ streams be used. For the other cases, the matrices are replaced by their first S columns. The term to be minimized in (2) can be expressed as

$$\begin{aligned} \mid\mid \mathbf{VD} - \hat{\mathbf{V}}_i \mid\mid_F^2 &= 2\text{tr}[\mathbf{I}] - \text{tr}\left[\hat{\mathbf{V}}_i^H \mathbf{VD} + (\hat{\mathbf{V}}_i^H \mathbf{VD})^H\right] \quad (5) \\ &= 2N - 2\text{tr}\left[\Re[\hat{\mathbf{V}}_i^H \mathbf{VD}]\right] \\ &= 2N - 2\Re\left[\sum_{k=1}^{N} \hat{\mathbf{v}}_{ik}^H \mathbf{v}_k e^{j\theta_k}\right] \quad (6) \end{aligned}$$

where $\mathbf{D} = \text{diag}(e^{j\theta_1}, e^{j\theta_2}, \ldots, e^{j\theta_N})$, $\hat{\mathbf{v}}_{ik}$ and $\mathbf{v}_k$ correspond to the k^{th} column of $\hat{\mathbf{V}}_i$ and $\mathbf{V}$, respectively. Minimizing (5) is equivalent to maximizing the second term in (6). It is easy to see that the optimal value of θ_k maximizing the summation in (6) is

$$\theta_k^{opt} = -\phi_k \qquad j = 1, 2, \ldots, N \tag{7}$$

where $0 \leq \phi_k < 2\pi$ is the phase of $\hat{\mathbf{v}}_{ik}^H \mathbf{v}_k$. ■

Proposition 1 results in the following optimal selection criterion in the Euclidean sense.

Selection Criterion - Optimal Euclidean (SC-OE) : The receiver selects $\mathbf{V}_L$ such that

$$\mathbf{V}_L = \underset{\hat{\mathbf{V}}_i \in \mathbb{V}}{\arg\min} \mid\mid \mathbf{VD}^{opt} - \hat{\mathbf{V}}_i \mid\mid_F^2. \tag{8}$$

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[1] E. Akay, E. Sengul, and E. Ayanoglu, "Bit interleaved coded multiple beamforming," *IEEE Trans. Commun.*, to appear.
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UC Irvine Center for Pervasive Communications and Computing

Graduate Fellowship Progress Report (Winter 2007)

Project name:	Cognitive Radio - Opportunistic and Reconfigurable Communication with Distributed Side Information
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Student:	Sudhir Srinivasa (sudhirs@uci.edu)
Date:	24 May 2007

Introduction:

The central idea in cognitive communications is to improve the utilization of the radio spectrum by dynamically adapting to spectrum availability. Recent research has proposed different interpretations of cognitive radio that underlay, overlay and interweave the transmissions of the cognitive user with those of the licensed users. Opportunistic communication with the interweave technique faces a multitude of challenges in the detection of primary systems and spectrum access, coexistence and sharing in multiuser environments.

Summary of Accomplishments:

In the past quarter, we submitted two conference papers [1][2], both to the IEEE Global Telecommunications Conference, 2007. We are actively working on journal papers associated with these two submissions.

In [1], we explore sensing based transmit power control in cognitive radio systems. We consider a cognitive radio system where the secondary transmitter varies its transmit power based on all the information available from the spectrum sensor. The operation of the secondary user is governed by its peak transmit power constraint and an average interference constraint at the primary receiver. Without restricting the sensing scheme (total received energy, or correlation, etc), we characterize the power adaptation strategies that maximize the secondary user's SNR and capacity. We show that, in general, the capacity optimal power adaptation requires decreasing the secondary transmit power from the peak power to zero in a continuous fashion as the probability of the primary user being present increases. Surprisingly, we find that that power control that maximizes the SNR is binary, i.e., if there is any transmission, it takes place only at the peak power level. Numerical results for common spectrum sensing schemes show that the SNR and capacity maximizing schemes are closely matched and will be identical when the sensing/observation time goes to infinity.

In [2], we explore the performance tradeoff between opportunistic and regulated access that is inherent in the design of multiuser cognitive radio networks. We consider a cognitive radio system with sensing limits at the secondary users and interference tolerance limits at the primary and secondary users. Our objective is to determine the optimal amount of spectrum sharing, i.e., the number of secondary users that maximizes the total deliverable throughput in the system. In the case of perfect primary user detection and zero interference tolerance at each of the primary and secondary nodes, we find that the optimal fraction of licensed users lies between the two extremes of fully opportunistic and fully licensed operation and is equal to the traffic duty cycle. For the more involved case of imperfect sensing and non-zero interference tolerance constraints, we provide numerical simulation results to study the tradeoff between licensing and autonomy and the impact of primary user sensing and interference tolerance on the deliverable throughput.

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Progress report on UWB research: Winter 2007

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***Abstract*—In the DS-UWB receiver, a pulse generator is needed to correlate the input pulse for synchronization. A flexible pulse generator was proposed and designed. In this pulse generator, a baseband gate pulse was generated with variable width and a frequency synthesizer was designed to provide dual carrier frequencies for upconversion.**

I. Introduction

In DS-UWB system [1], in order to avoid interference with available IEEE 802.11a system at 5GHz, the 7.5GHz bandwidth is divided into two bands: higher band (6GH~10GHz) and lower band (3GHz~5GHz). One challenge with the specification of spectrum in DS-UWB is to design a pulse signal which exactly has a dual band characteristic. Normally, current available designs [2-3] generate the pulse which only works on lower band, because of the difficulty to go higher band. In addition, most of the pulse generators are designed based on filtering a wideband signal. Therefore, they are not suitable for flexible design, which is another reason why only one band is chosen. In our recent work, a flexible pulse generator was designed and simulated to be suitable for both lower band and higher band separately.

II. Method of Pulse Synthesis

Frequency synthesizer

The frequency synthesizer shown in Fig. 1 includes 8GHz VCO, Injection Locking Frequency Divider (ILFD), CMOS static divider, conventional Frequency Phase Detector (FPD), Low Pass Filter (LPF) and a low-jitter Charge Pump (CP). In order to increase the dynamic performance of the PLL, a wider loop bandwidth is targeted for fast setting time. A high frequency reference signal was applied to the PLL to reduce the error by using a continuous system simulating a discrete one. A complementary LC VCO was designed for better phase noise and also easily interfaces with the next stage. To provide the same tuning property of VCO and ILFD, the loading capacitors of VCO and ILFD tanks are carefully designed. For the divider, normally CMOS static divider is preferred because of low power consumption. However, if different phases need to be generated like I,Q signals. CML divider is a better choice for less jitter during the clock transition. Since the input of the PFD is a CMOS signal, CML to CMOS converter is also designed for interconnection. The PLL system simulation is performed under CPPSim, an easy tool provided by MIT high speed circuits and systems group. In our design, the loop bandwidth is chosen to be 2MHz, the calculated capacitors and resistor are reasonable for on-chip integration.

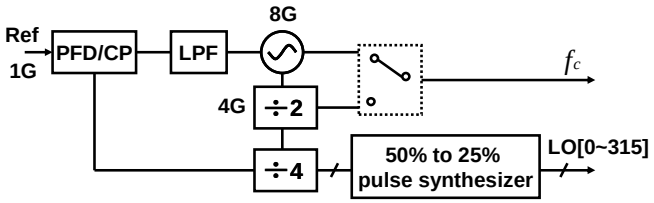

Fig. 1. Block diagram of pulse generator

III. Simulation Results

The step response of the PLL is simulated by CPPSim (Fig. 2). The PLL is a second order type II system, which contains a resistor series with a capacitor then parallel with a current injection capacitor. PLL initial start up time is much longer than the settling time because of the initial state for charge pump. In order to make sure the PLL is always trying to lock, a wider tuning range of VCO and ILFD are needed. A transient simulation is running to make sure the PLL won't falls locking at the startup. The simulation result is shown in Fig. 3

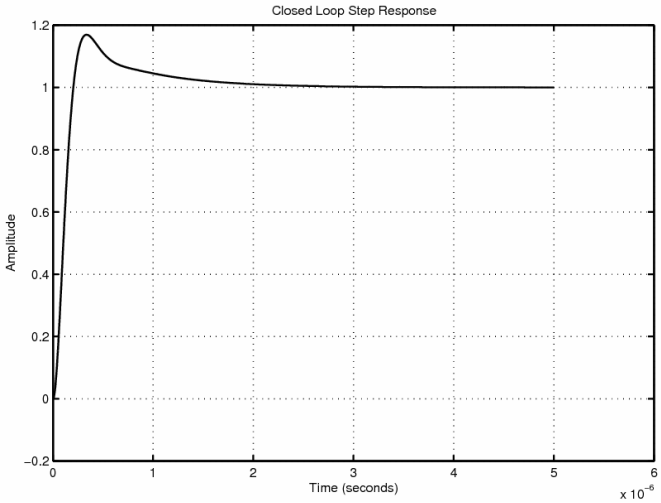

Fig. 2. PLL step response

In the lock condition shown in Fig. 4. There is a static error between divider output and reference signal. Since we care only frequency in this PLL, this won't cause any other problem.

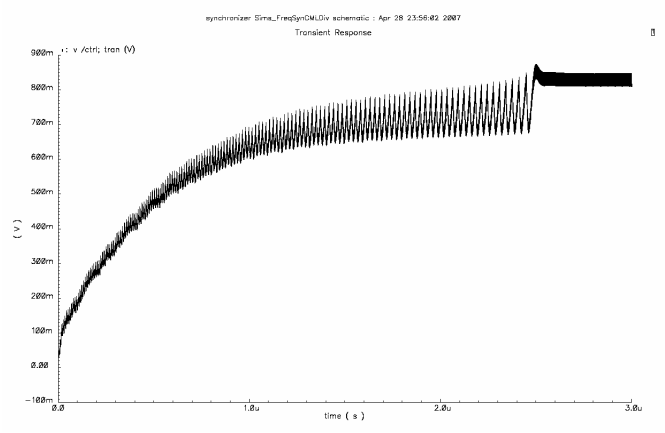

Fig. 3. Control voltage in the PLL

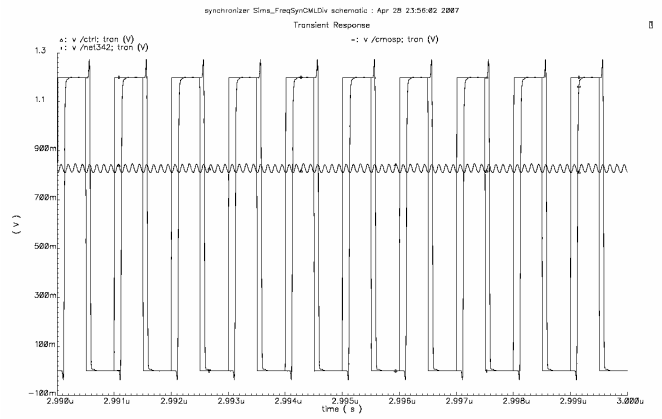

Fig. 4. Transient simulation of PLL

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