Circuit and Systems

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Possible Research Collaboration

- Exploring unique opportunity with mutual benefit
- Strong collaborative research with High-Tech Companies in Southern California
  - Numerous research grants and gifts since 2000
  - Published several joint papers with researchers
- Possibility of accessing to CMOS MPW tape-outs
- Proximity of high-tech companies with UC Irvine make this current collaboration much stronger than ever before

Possible Research Collaboration

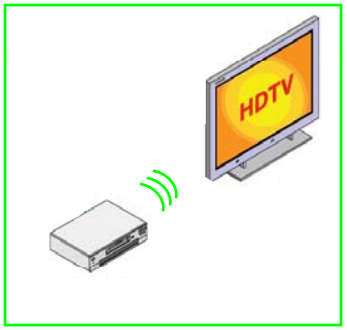
- Will sustain excellence in circuit/system design research at UC Irvine
- Will significantly impact the quality of research in the wireless/wireline area at UCI, not to be found in any research groups at other US universities

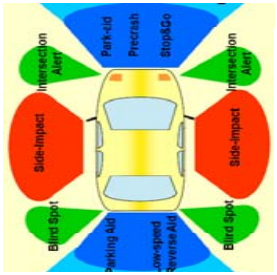
Practical Ways for Implementation

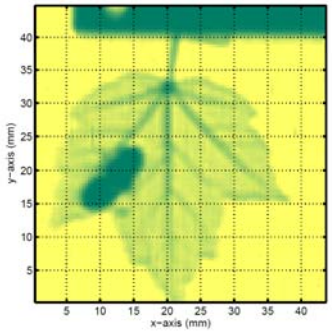
- Giving strict access of nanoscale CMOS process
- Prepare quarterly report about the research progress
- Tape-out twice a year, with chip size no more than $4 \times 4 mm^2$

Summary

- Design and implementation of novel circuits and systems for sensing, (medical) imaging, and communications







- 13 student posters showcasing the research under the circuits and systems trust

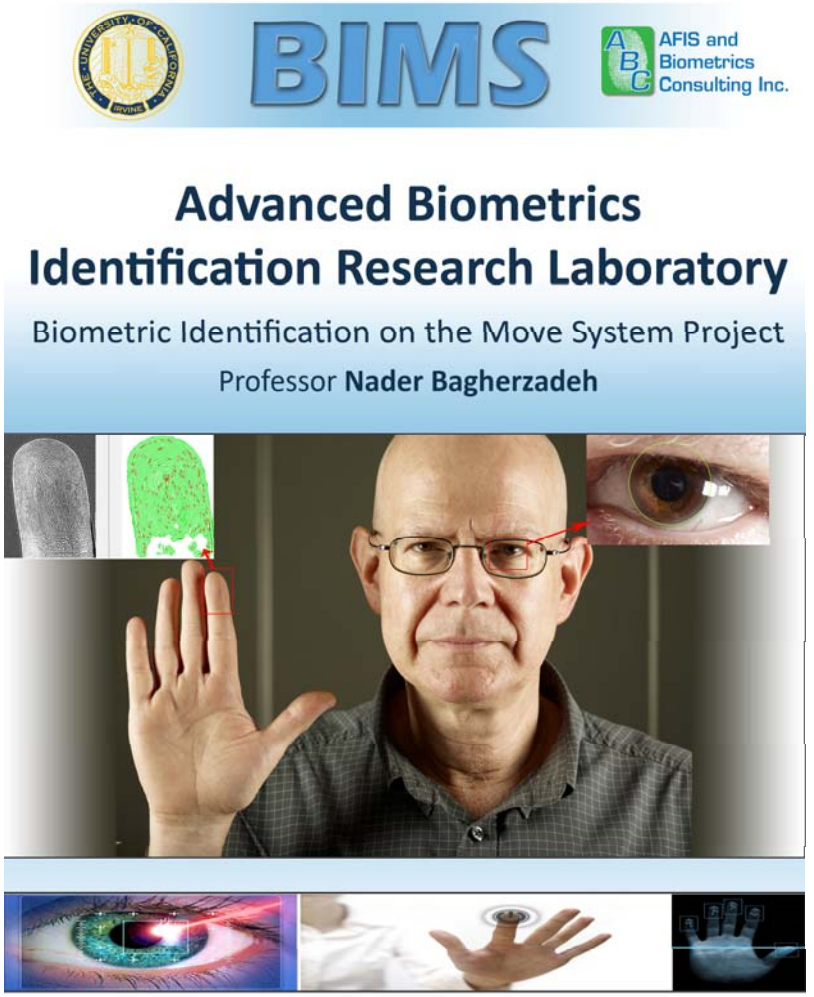
Nader Bagherzadeh

CPCC, Dept. of EECS, Irvine, CA

- Biometrics
- Network-on-Chip
- Wireless Sensor Network

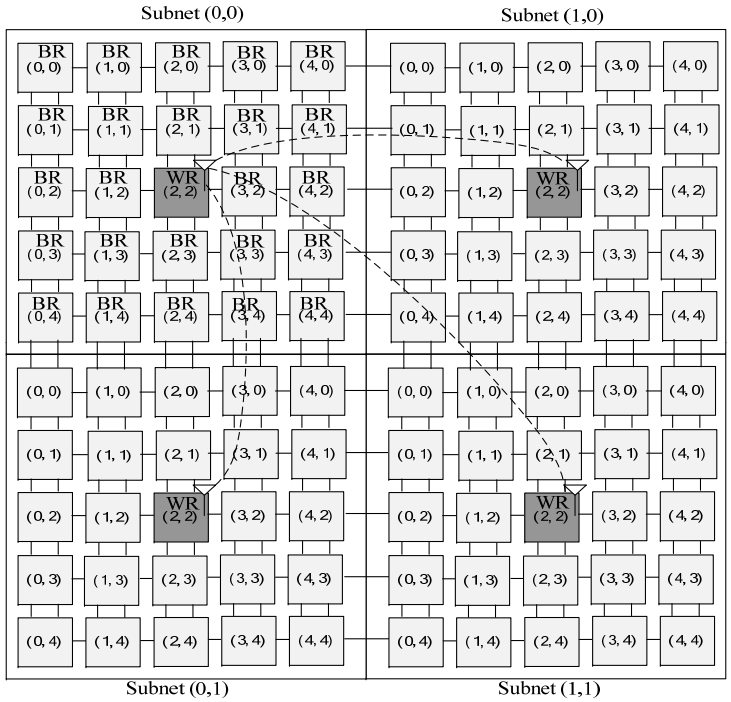
BIMS

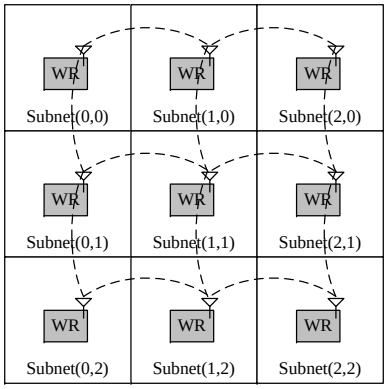
- Biometric Identification on the Move System, BIMS
  - Stage one: Enrollment of high quality fingerprint, iris and face.
  - Stage two: Identification by capturing face, iris and fingerprint from distance:
    - Iris Capturing: Near Infra-red high resolution camera(s)
    - Face Capturing: Multiple pose cameras
    - Fingerprint: Fingerprint on the Move Scanner by moving a hand over a surface.



Wireless Network-on-Chip

- Use a myriad of communication links for on chip networking
- Congestion-aware routing mechanism to balance traffic load
- Quality-aware routing algorithm to intelligently utilize resources
- Fault-tolerance achieved by adaptive routing among hybrid networks
- Hybrid routers (optical, wired and wireless)
- Hardware/software co-design for heterogeneous platforms using hybrid network-on-chip technology





- Development of Wireless Sensor Network (WSN) for detection of pollutant and illicit material by monitoring Raman scattering using laser based sources.

- Areas of focus are:
  - Low power platform design
  - Sensor integration
  - Networking

Ahmed M. Eltawil

Wireless Systems and Circuits Laboratory
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http://newport.eecs.uci.edu/~aeltawil/
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- Visualizing Memory Behavior
- Cognitive Power Management
- Directional MEMS Antennas

Sample of Active Projects

- Software defined radios for public safety applications
  - Architectural design of scalable SDR platforms with minimum power consumption.
- Power management for wireless and multimedia applications.*
  - Cross-layer power management approaches to manage design margins and process variation effects in highly scaled technologies.
  - Focus on low power error tolerant cache and memory system architectures.
- Low power VLSI architectures for key building blocks such as:
  - Sphere decoding for MIMO systems
  - Programmable FEC cores
  - Channel estimation
  - Etc.

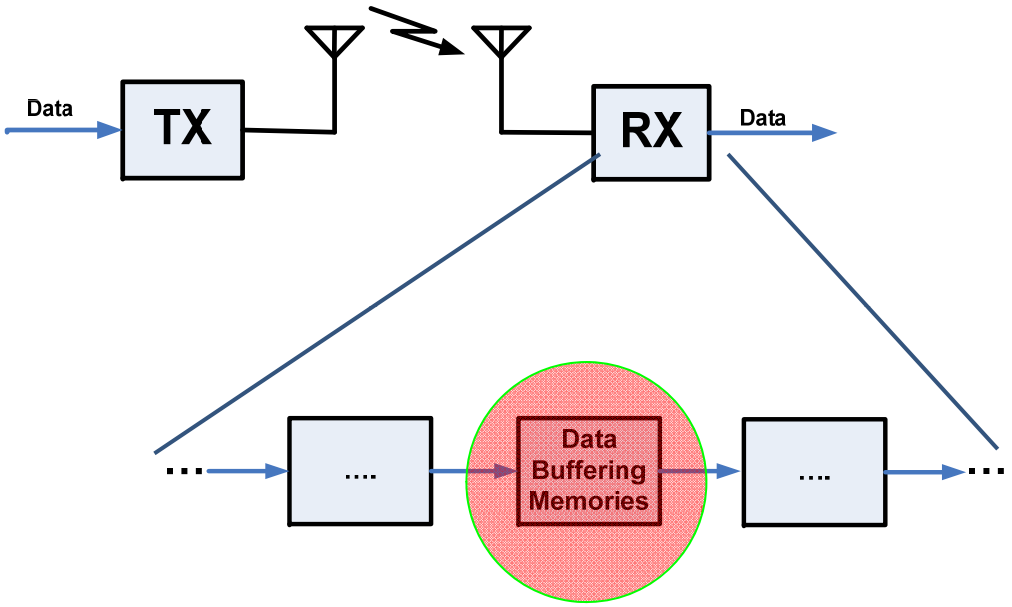
* Collaboration with professor Fadi Kurdahi at UCI

Cognitive Power Management

Developed runtime power management algorithms that utilize extra channel "slack" to reduce power by applying aggressive voltage scaling on memories while allowing the hardware to "fail" in a controlled manner.

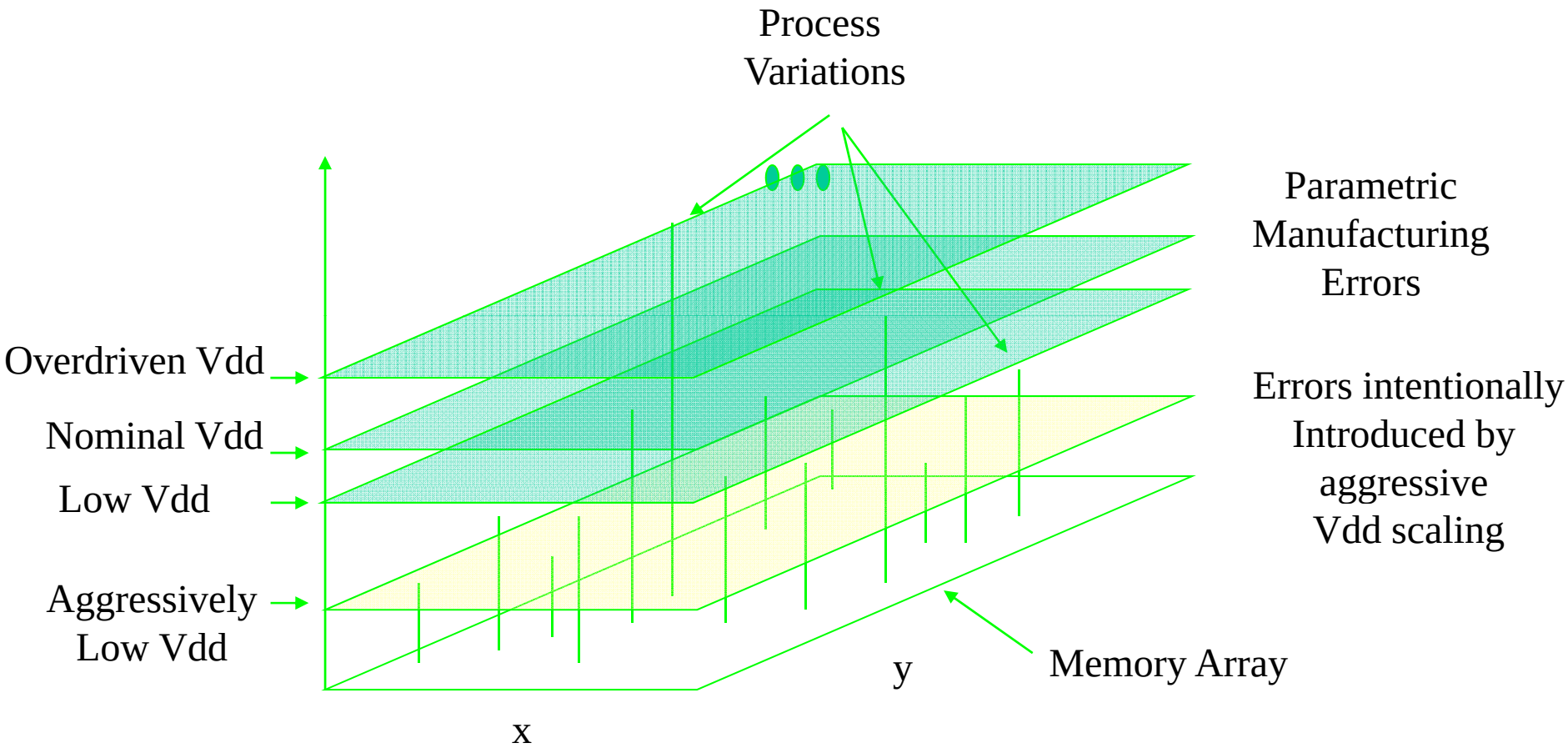
$BER_{total} = BER_{channel} + BER_{hardware}$

Power savings > 40%



- **Consume a large portion of the design area**
- **Store raw soft bit values that have multiple levels of redundancy:**
  1. **At the algorithmic level, coding redundancy exists**
  2. **Most of the time, the receiver experiences a relatively higher SNR than the minimum required for demodulation**

Visualizing Memory Behavior

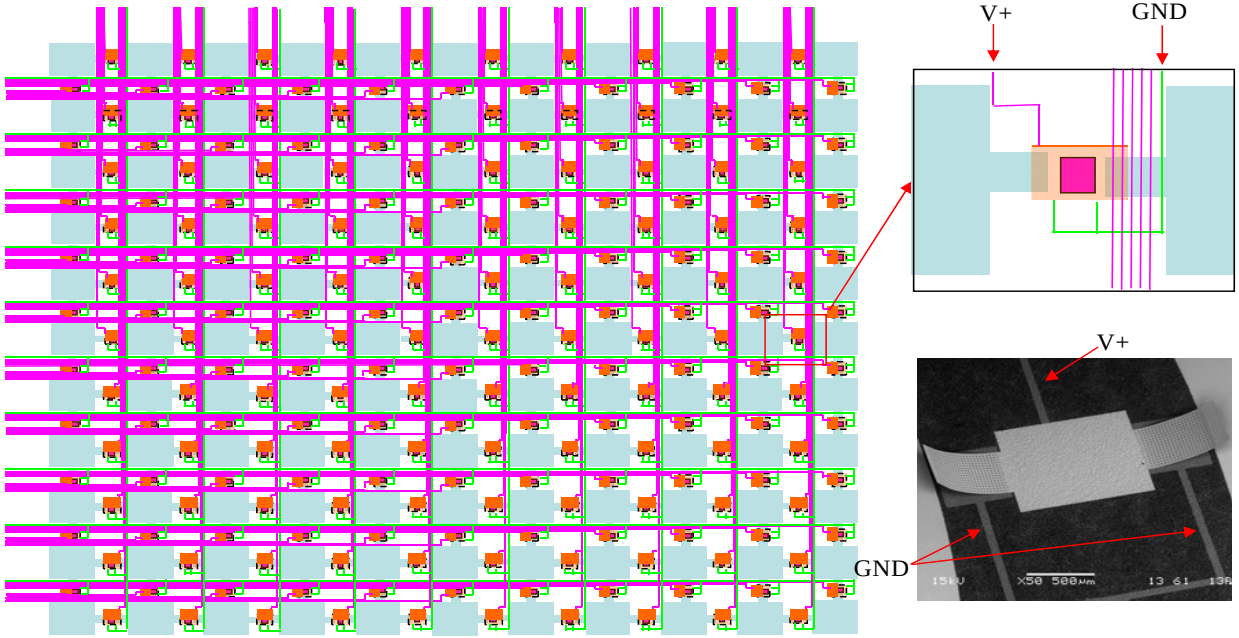


Manage power jointly based on wireless channel quality and buffering memory voltage

Directional MEMS Antennas

MEMS Integrated Multifunctional Reconfigurable Antenna (MRA)

- A single antenna dynamically providing
  - Multi-frequency
  - Multi-polarization
  - Variable Radiation Pattern with beam tilting capabilities
  - ***Lower number of RF chains ⇒ Lower Power***

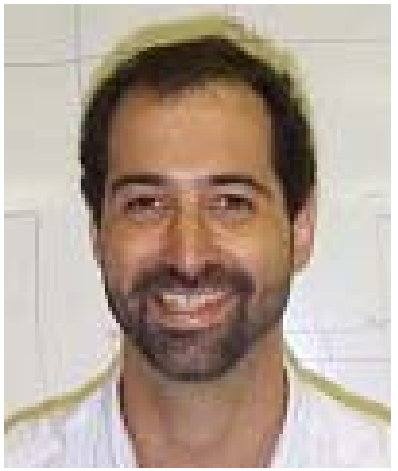


MRA ARCHITECTURES: *MRA Pixel patch*

Modes of operation: *Polarization; LP, RHCP, LHCP. Frequency; 700, 800, 2400, 4900 MH, Radiation Pattern; 30º tilt angle*

Collaboration with Professor Bedri Cetiner at Utah State University

Michael Green



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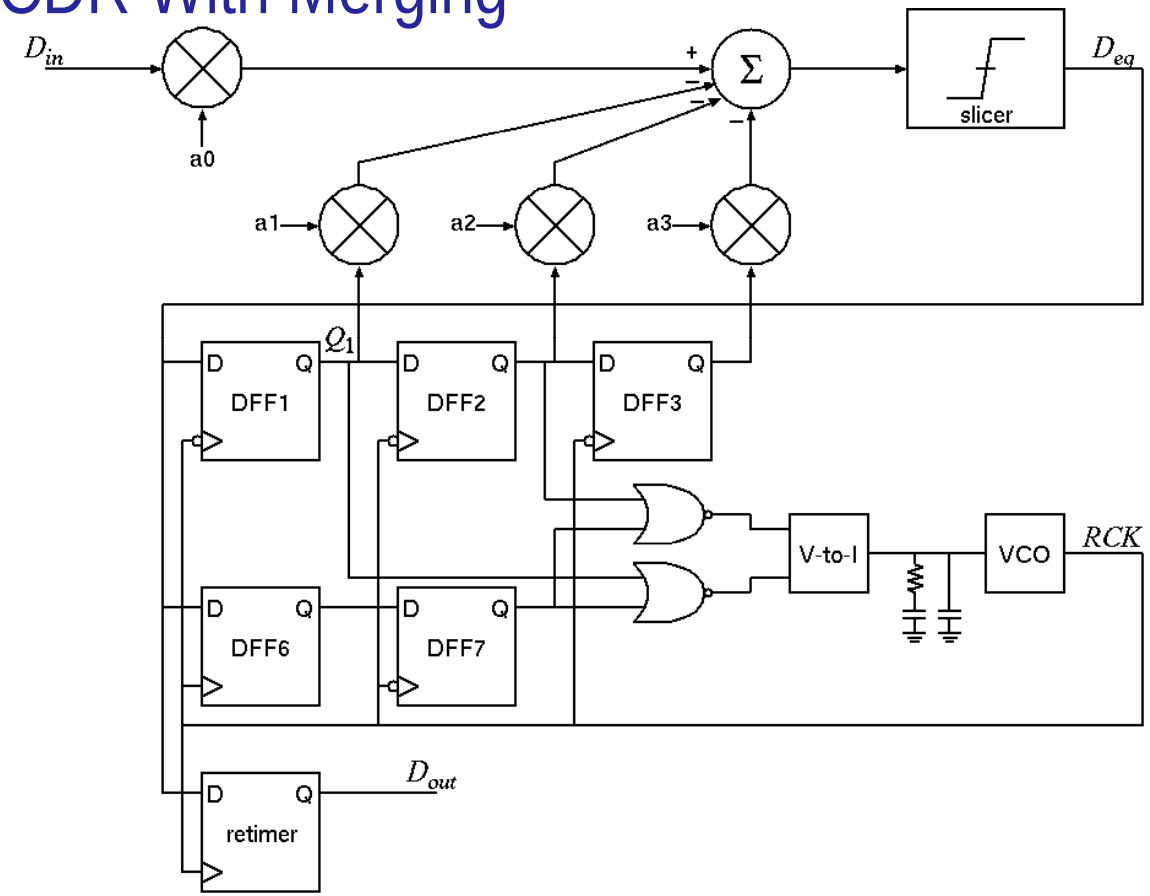
☞ CMOS Design Techniques for Multi-Gb/s Broadband Communication Circuits

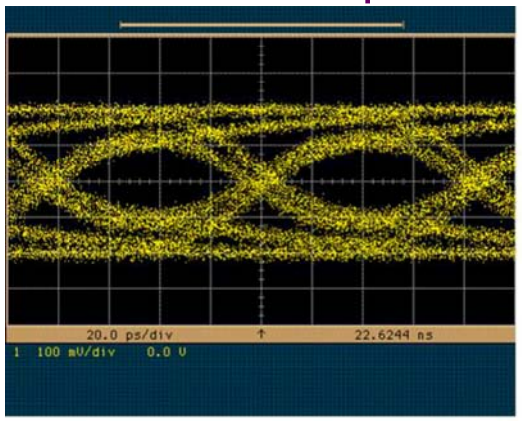
DFE and CDR With Merging



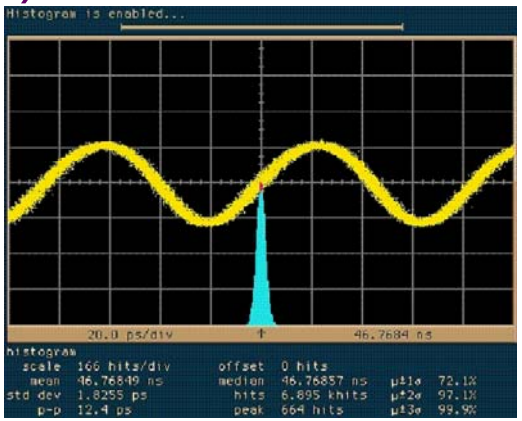
- Merging results in less power dissipation and less loading on the recovered clock signal.

Equalizer + CDR Operation (2)

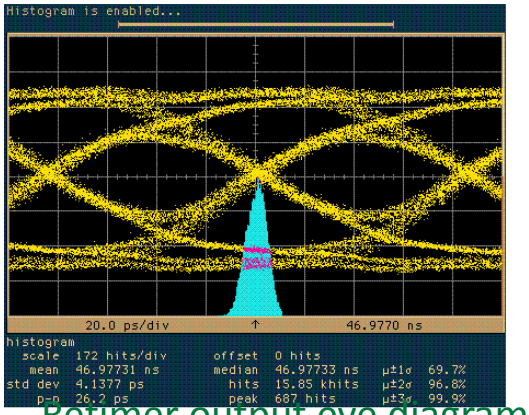
2.4 m cable



Cable output eye diagram.

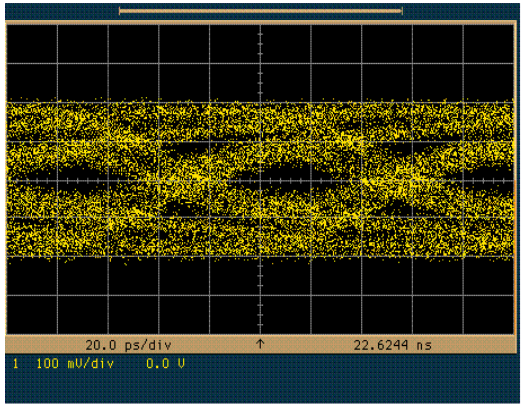


Recovered clock
RJ = 1.83 ps rms

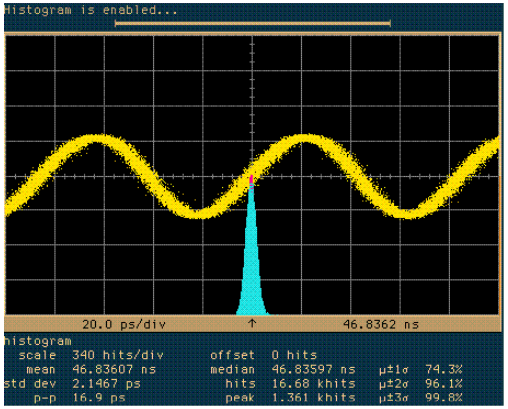


Retimer output eye diagram
Jitter = 4.14 ps rms

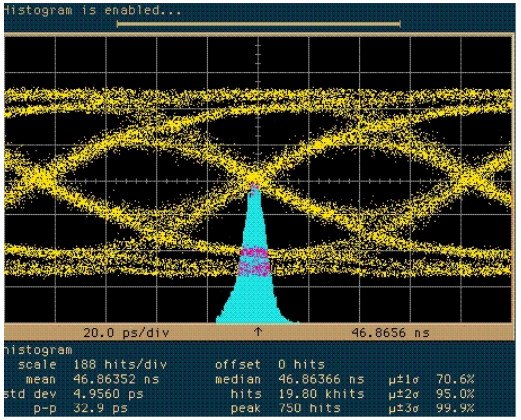
3.6 m cable



Cable output eye diagram.

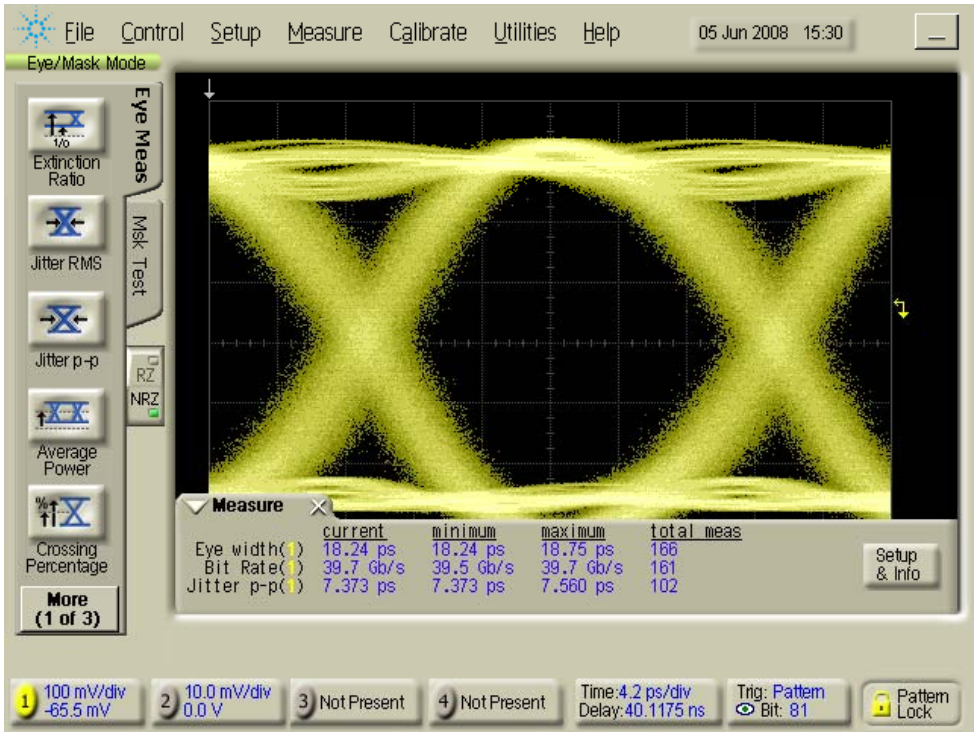


Recovered clock
RJ = 2.15 ps rms



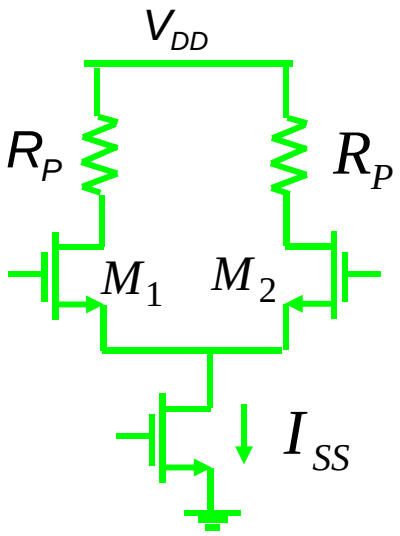
Retimer output eye diagram
Jitter = 4.96 ps rms

Measured 40 Gb/s Output



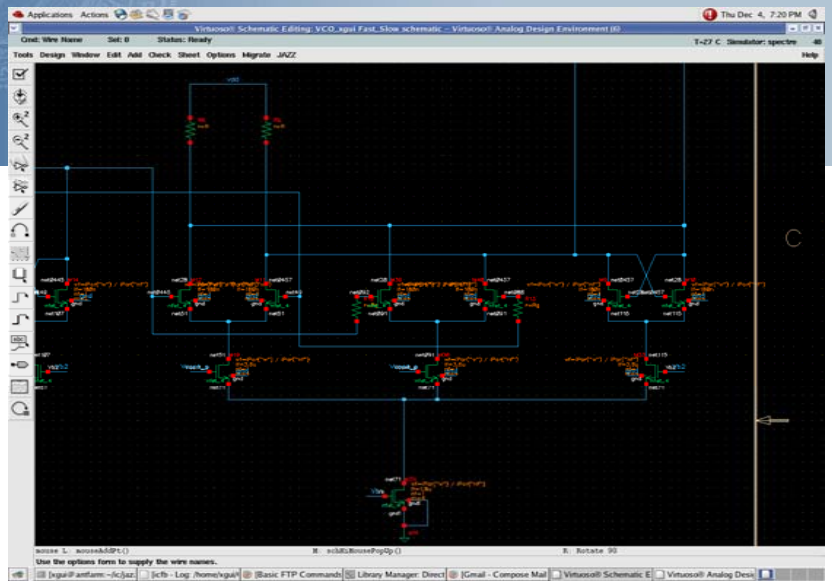
40Gb/s MUX output (Differential) with 450 mV differential peak-to-peak vertical eye opening and 1.14 ps rms jitter

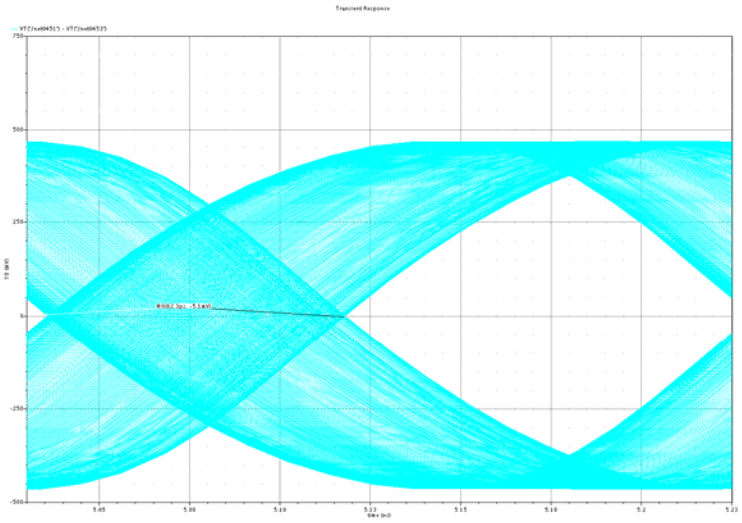
Design of High-PSRR VCOs

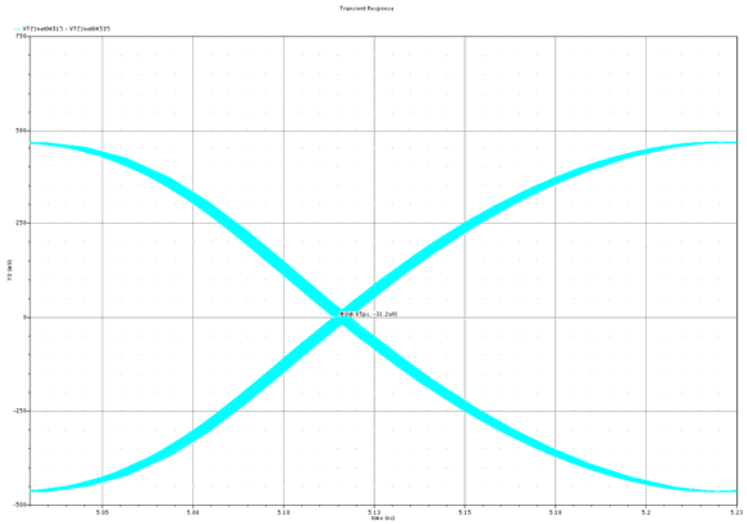


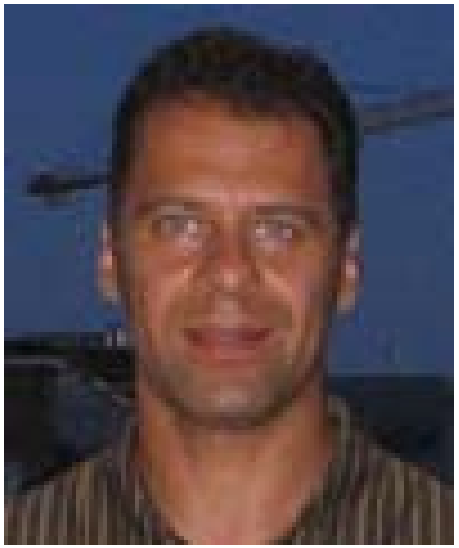
Effect of Power Supply Noise

- *Variation on Vdd causes variation of the dc operating point, changing the dc operating point.*
- *As a result, output impedance of M1 and M2 varies, changing the effective load resistance.*
- *Finally, self-oscillation frequency deviates.*









Payam Heydari

Nanoscale Communication IC Labs

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- Silicon-Based Radar-on-Chip
- THz Active and Passive Imaging
- High-Speed Low-Power Analog-to-Digital Converter
- Broadband Integrated Circuits

Research Areas

Nanoscale Communication IC Labs

http://ncic.eng.uci.edu

High-Speed Broadband

- Distributed Amplifiers/Buffers (DAs)
- 6-bit 10GS/sec Low-Power ADC in 130nm CMOS
- Novel BW-Enhancing Techniques for Broadband IC's

RF/Millimeter-Wave

- Multi-Antenna TRX Design
- (Sub)-Millimeter-Wave ICs for Imaging, Sensing, and Communications
- Ultra-Low Power RFIC's for Biomedical Applications

- Designed and fabricated more than 40 RF/Analog silicon chips since 2002
- Filed 10 patents since 2002; three were issued

(Sub)-Millimeter-Wave Applications

94GHz

75 GHz

24GHz
Automotive Short-range Radar

60GHz
Gbps WLAN/WPAN

77/79GHz
Future Automotive Short-range Radar

Passive Imaging

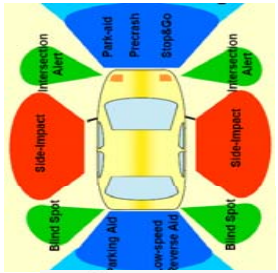
120GHz
Broadband Wireless Communication

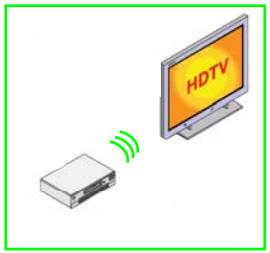
140GHz
Passive/Active Imaging

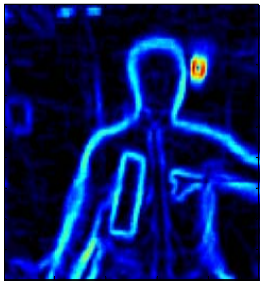
0.3 – 3 THz
THz Imaging - Spectroscopy

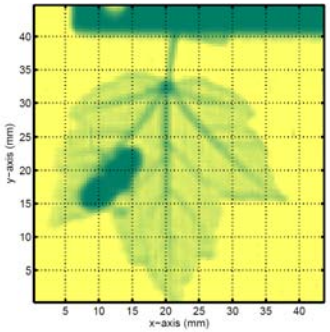
GHz

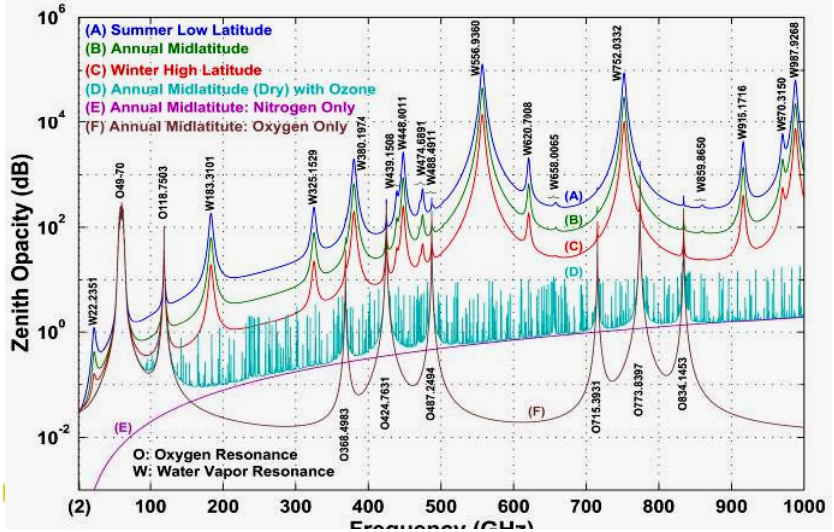
22 29 57 64 77 81 95 115 140

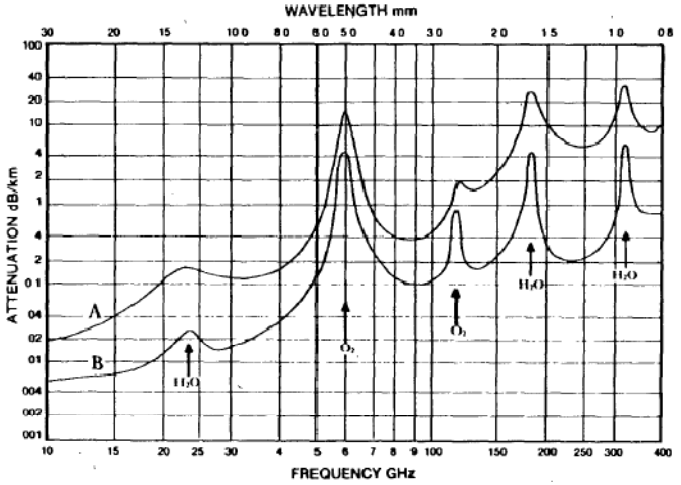






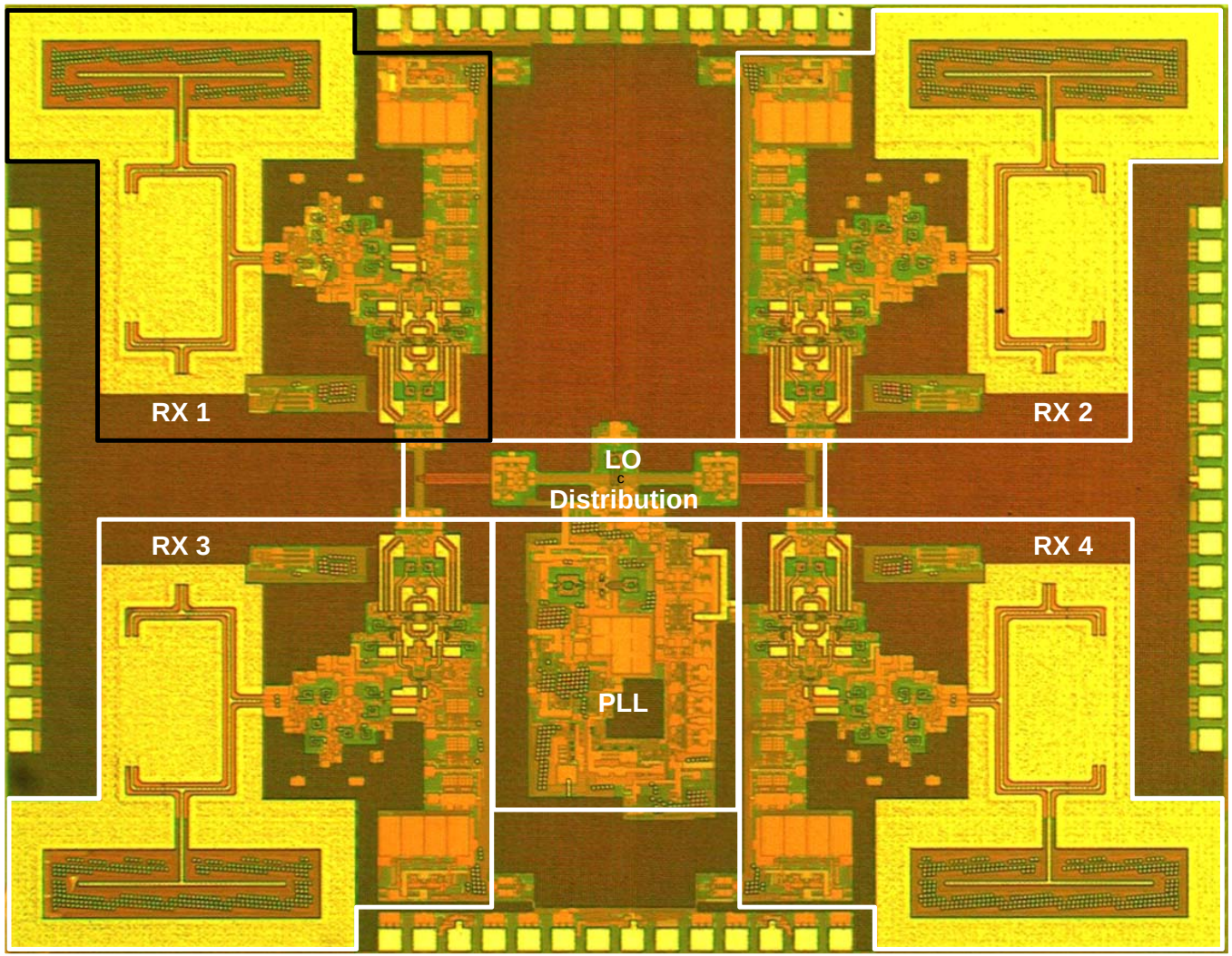






Coming Attractions (1)

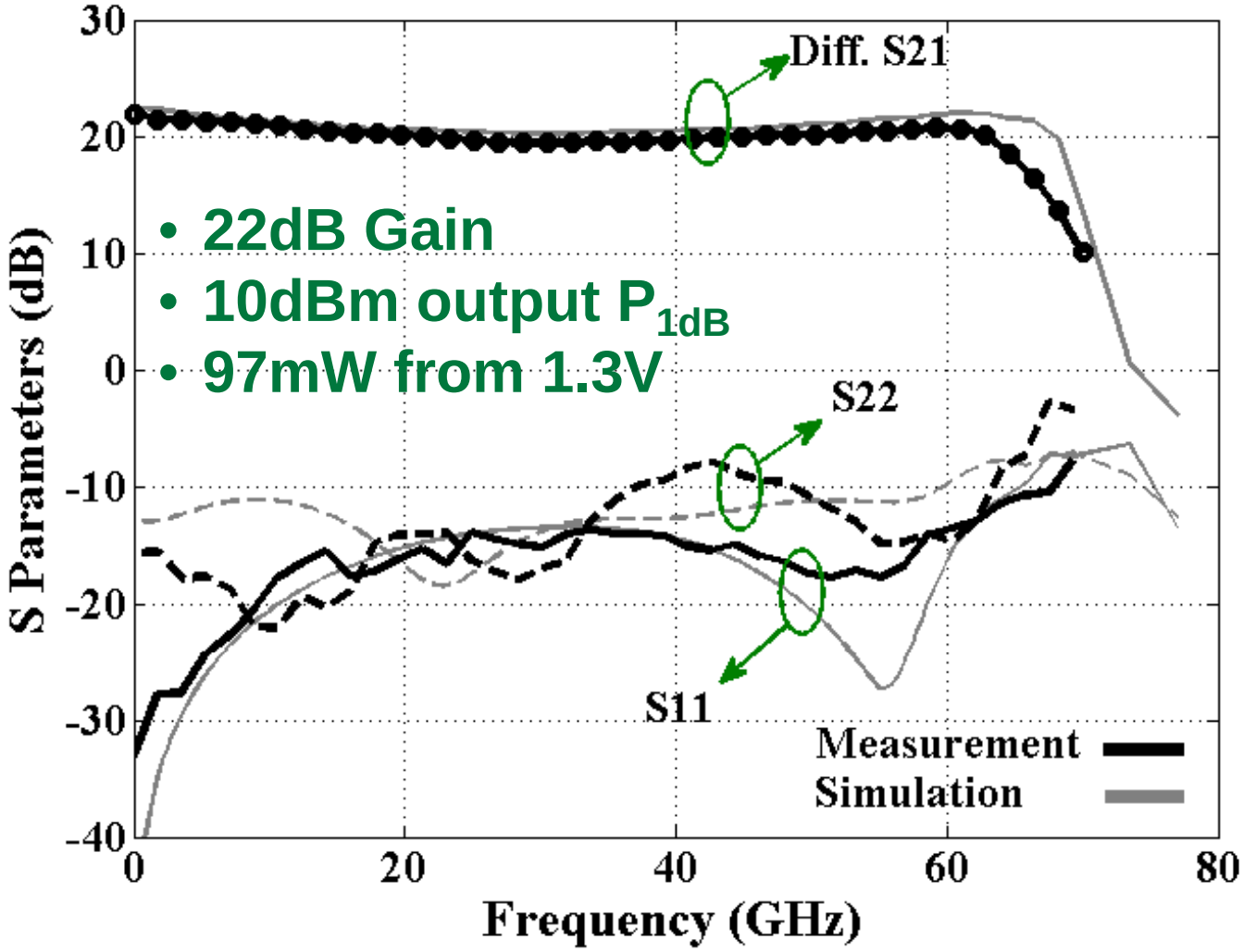
A Fully Integrated 100GHz Focal-Plane Array Passive Imager



Researchers: Zhiming Chen and Chun-Cheng Wang

Coming Attractions (2)

A CMOS Highly Linear Distributed Amplifier

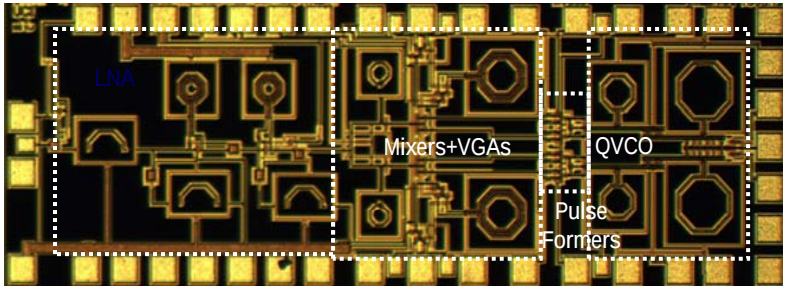


- 22dB Gain
- 10dBm output P_{1dB}
- 97mW from 1.3V

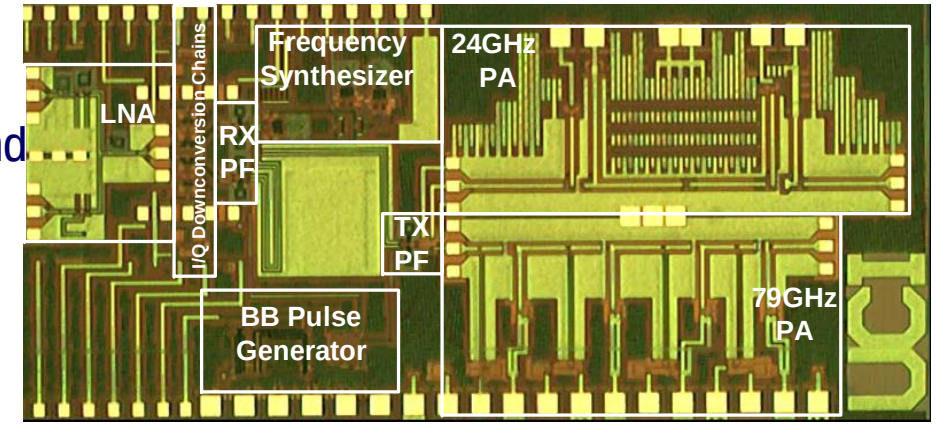
Researcher: Amin Jahanian

Highlights (1)

- Designed and tested the first CMOS 22-29GHz automotive radar receiver front-end in TSMC 180nm
- Results appeared in CICC 2007 and T-MTT Aug. 2009
- Measurement done in NCIC Lab



- The first dual-band architecture for millimeter-wave 22-29 GHz / 77-81GHz TRX was designed and fabricated in BiCMOS 180nm technology.
- Results appeared in ISSCC 2009 and JSSC Dec. 2009.



- A carrier-less RF-correlation-based IR-UWB TRX front-end in 130nm CMOS was designed.
- Occupying 6.4mm^2 chip area, the TRX achieves a data rate of 2Gbps and RX sensitivity of -64dBm with a BER of 10^{-5}.
- Results appeared in RFIC Symp. 2009 and TMTT April 2011

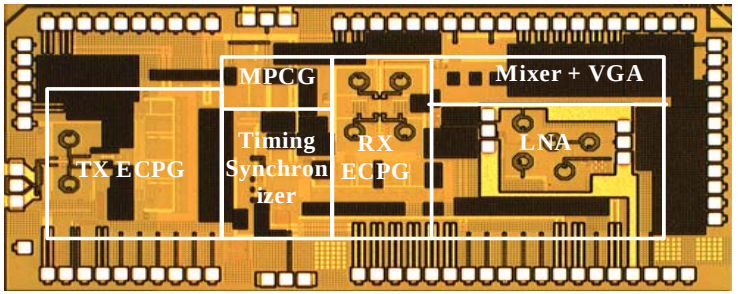
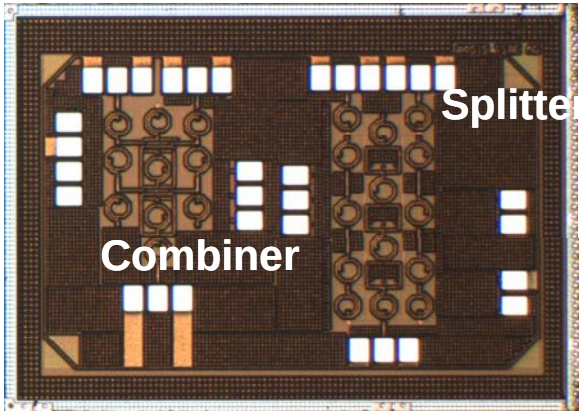


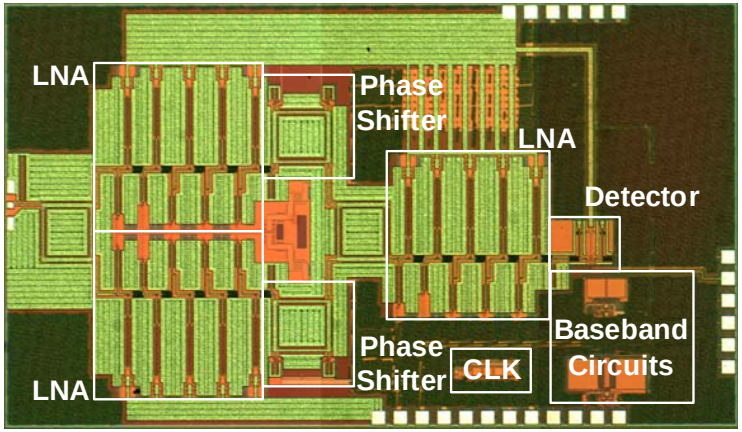
Fig. 7 Die micrograph

Highlights (2)

- Designed and tested CMOS active power combiner/splitter for multi-antenna transceivers
- The results appeared in July issue of JSSC 2007
- Measurement done in NCIC Lab



- The first reported integration of a silicon-based 94-GHz passive imaging receiver with on-chip baseband circuitry.
- The paper was presented RFIC Symp. 2010.



Student Posters

- *An 85-95.2 GHz Transformer-Based Injection-Locked Tripler (ILFT) in 65nm CMOS*
  Zhiming Chen and Payam Heydari
- *A Novel Highly Inductive, Low Loss Slow Wave CPW Structure*
  Byung-Kwan Chun, Peyman Nazari, Payam Heydari
- *A W-band CMOS Receiver Chipset for MMW Radiometer Systems*
  L. Zhou, C.-C. Wang, Z. Chen, and P. Heydari
- *A 2.4 GHz Highly Linear LNA*
  Eric Middleton, Payam Heydari
- *Wide-IF-Band CMOS Mixer Design*
  P.-Y. Chiang and Payam Heydari
- *Distributed Amplifier with GBW/Linearity Enhancement*
  Amin Jahanian and Payam Heydari
- *A Design of Broadband D-band On-chip Antennas*
  Zheng Wang, Zhiming Chen, Payam Heydari